

Support Group Application Note

*Number: 035*

*Issue: 1*

*Author: D J Bell*



## BBC Master 128 Cartridge Interface

This application note details the Cartridge Interface on the Master Series machines with differences for operation with the Electron Plus 1 noted where relevant.

Applicable

Hardware :

BBC Master 128

Related

Application

Notes:

Copyright © Acorn Computers Limited 1992

Every effort has been made to ensure that the information in this leaflet is true and correct at the time of printing. However, the products described in this leaflet are subject to continuous development and improvements and Acorn Computers Limited reserves the right to change its specifications at any time. Acorn Computers Limited cannot accept liability for any loss or damage arising from the use of any information or particulars in this leaflet. ACORN, ECONET and ARCHIMEDES are trademarks of Acorn Computers Limited.

Support Group  
Acorn Computers Limited  
Acorn House  
Vision Park  
Histon  
Cambridge CB4 4AE

## Abbreviations

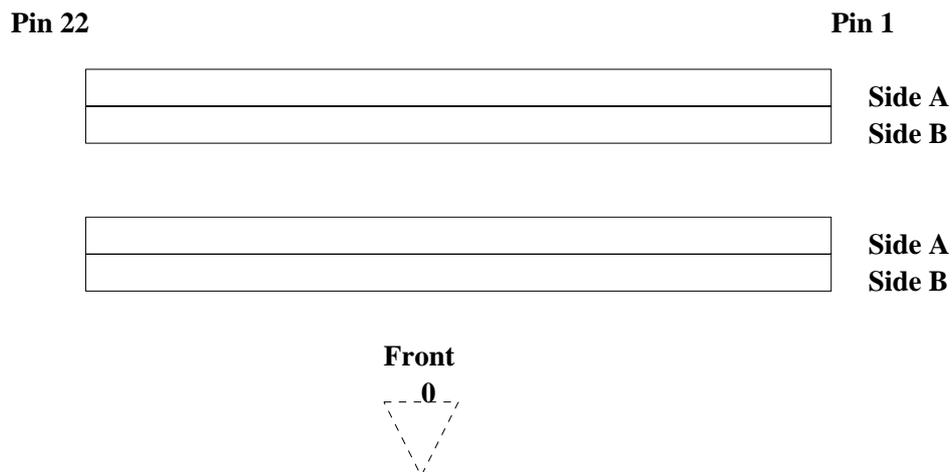
Abbreviations are used in this Note as follows:

A/L	Active Low
O/C	Open Collector output
CMOS	Complementary-symmetry Metal Oxide Semiconductor
CPU	Central Processor Unit ie, the microprocessor
TTL	Transistor-Transistor Logic
&	A hexadecimal number follows
n	As a signal prefix means Active Low output (A/L)
PCB	Printed Circuit Board
NMOS	Nitride-layer Metal Oxide Semiconductor

## Cartridge Orientation

The cartridge pinning in the Master Series machine is arranged as follows:

**Viewed from above**



Components are normally mounted onto Side A of the PCB within the cartridge.

## Pinout

Pins are described viewed from "within" the cartridge ie, an "Input" is an input to the cartridge. An "output" is an output to the computer.

### SIDE A

- |   |  |                            |
|---|--|----------------------------|
| 1 | +5V - Logic power supply.<br>150mA max in a Master with co-processor fitted and with disk drives.<br>50mA max in an Electron Plus 1.   |                            |
| 2 | nOE - Output Enable.<br>Low during PH12 period of system clock. It is intended to switch on the output buffers of cartridge memory devices. It is not guaranteed low at other times. | Input from A/L CMOS level. |

- 3 nRST - System Reset. Input from A/L CMOS level.  
Low during a system reset. It is not synchronised to any clock.
- 4 CSRW - Chip Select - Read/Write. Input from CMOS level.  
Master - Changes function according to the memory region that the CPU is addressing.  
During accesses to &FC00 through &FEFF it is equivalent to the CPU Read/Write line during nPH12. For all other accesses it is an Active High chip select for memory devices.  
It is not guaranteed low at other times.  
Electron - CPU Read/Write line.
- 5 A8 - Address line 8. Input from TTL level.
- 6 A13 - Address line 13 Input from TTL level.
- 7 A12 - Address line 12 Input from TTL level.
- 8 PH12 - CPU clock. Input from CMOS levels.  
Computer's PH12 output.
- 9 -5V - Negative supply voltage.  
20mA max. This -5V may not be available on all Acorn Cartridge Interfaces. To ensure compatibility, negative voltages should be generated within the Cartridge if required.
- 10 CSYNC/MADET  
Master - There are two functions dependent upon link 12 in the computer:  
E/nB - the default function. It enables cartridges to know which machine they are plugged into. It is connected to 0V in the Master (and unconnected in the Electron). Link 12 is set to position B.  
CSYNC - Composite Sync. Input from TTL levels.  
System Vertical & Horizontal sync is made available fro Genlock use. Set Link 12 to position B.  
Electron - Unconnected.
- 11 RNW/READY  
Master -  
R/W - Data Direction Control. Input from TTL levels  
System data buffer direction control. If low, cartridges are being written to; if high and selected, they may drive the bus during PH12.  
Electron -  
READY - CPU wait state control O/C A/L output  
When driven low, this line will cause the CPU to extend it's cycle until READY is released.  
Only works with CMOS CPUs. Will only work on READ cycles with NMOS CPUs.
- 12 nNMI - Non-maskable Interrupt. O/C A/L output.  
Connected to the system NMI line.
- 13 nIRQ - Interrupt request. O/C A/L output.  
Connected to the system IRQ line.



## SIDE B

1	+5V - Logic power supply. 150mA max in a Master with co-processor fitted and with disc drives. 10mA max in an Electron Plus 1.	
2	A10 - Address line 10.	Input from TTL levels.
3	D3 - Data bus line 3.	Input/Output TTL levels.
4	A11 - Address line 11.	Input from TTL levels.
5	A9 - Address line 9.	Input from TTL levels.
6	D7 - Data bus line 7.	Input/Output TTL levels.
7	D6 - Data bus line 6.	Input/Output TTL levels.
8	D5 - Data bus line 5.	Input/Output TTL levels.
9	D4 - Data bus line 4.	Input/Output TTL levels.
10	nOE2/LPSTB - O/P Enable/Light Pen Strobe. <u>Master</u> - With link 21 removed in the computer, this pin provides a connection between the two cartridges. With the link in place, the pin forms a connection to a pull-up resistor in the computer to +5V. The connection is also made to the CRTIC Light-Pen Strobe and interrupt structure. <u>Electron</u> - This provides an additional A/L enable for ROMs in the Electron. This corresponds to ROM position 13 and responds quickly to Service Calls. It is low during the A/L portion of PH12. It is not guaranteed high at other times.	Input from TTL levels.
11	BA7 - Buffered address line 7. <u>Master</u> - This line holds addresses valid for 125nS after PH12 goes low. <u>Electron</u> - This is not buffered nor held valid for an extended period in the Electron.	Input from TTL levels.
12	BA6 - Buffered address line 6. see pin 11.	Input from TTL levels.
13	BA5 - Buffered address line 5. see pin 11.	Input from TTL levels.
14	BA4 - Buffered address line 4. see pin 11.	Input from TTL levels.
15	BA3 - Buffered address line 3. see pin 11.	Input from TTL levels.
16	BA2 - Buffered address line 2. see pin 11.	Input from TTL levels.
17	BA1 - Buffered address line 1. see pin 11.	Input from TTL levels.

---

18	BA0 - Buffered address line 0 see pin 11.	Input from TTL levels.
19	D0 - Data bus line 0.	Input/Output TTL levels.
20	D2 - Data bus line 2.	Input/Output TTL levels.
21	D1 - Data bus line 1.	Input/Output TTL levels.
22	0V - Zero volts. Digital signal Earth return.	