MOTOROLA
SEMICONDUCTORS
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MC6845

MOS
(N-CHANNEL, SILICON-GATE)

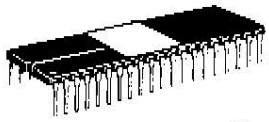
CRT CONTROLLER (CRTC)

CRT CONTROLLER (CRTC)

The MC6845 CRT controller performs the interface between an MPU and a raster-scan CRT display. It is intended for use in MPU-based controllers for CRT terminals in stand-alone or cluster configurations.

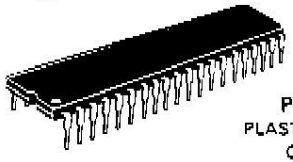
The CRTC is optimized for the hardware/software balance required for maximum flexibility. All keyboard functions, reads, writes, cursor movements, and editing are under processor control. The CRTC provides video timing and refresh memory addressing.

- Useful in Monochrome or Color CRT Applications
- Applications Include "Glass-Teletype," Smart, Programmable, Intelligent CRT Terminals; Video Games; Information Displays
- Alphanumeric, Semi-Graphic, and Full-Graphic Capability
- Fully Programmable Via Processor Data Bus. Timing May Be Generated for Almost Any Alphanumeric Screen Format, e.g., 80 × 24, 72 × 64, 132 × 20
- Single +5 V Supply
- M6800 Compatible Bus Interface
- TTL-Compatible Inputs and Outputs
- Start Address Register Provides Hardware Scroll (by Page or Character)
- Programmable Cursor Register Allows Control of Cursor Format and Blink Rate
- Light Pen Register
- Refresh (Screen) Memory May be Multiplexed Between the CRTC and the MPU Thus Removing the Requirements for Line Buffers or External DMA Devices
- Programmable Interlace or Non-Interlace Scan Modes
- 14-Bit Refresh Address Allows Up to 16K of Refresh Memory for Use in Character or Semi-Graphic Displays
- 5-Bit Row Address Allows Up to 32 Scan-Line Character Blocks
- By Utilizing Both the Refresh Addresses and the Row Addresses, a 512K Address Space is Available for Use in Graphics Systems
- Refresh Addresses are Provided During Retrace, Allowing the CRTC to Provide Row Addresses to Refresh Dynamic RAMs
- Pin Compatible with the MC6835



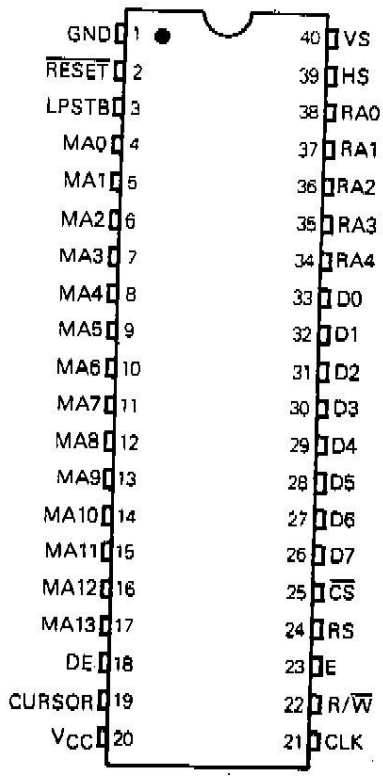
L SUFFIX
CERAMIC PACKAGE
CASE 715

S SUFFIX
CERDIP PACKAGE
CASE 734



P SUFFIX
PLASTIC PACKAGE
CASE 711

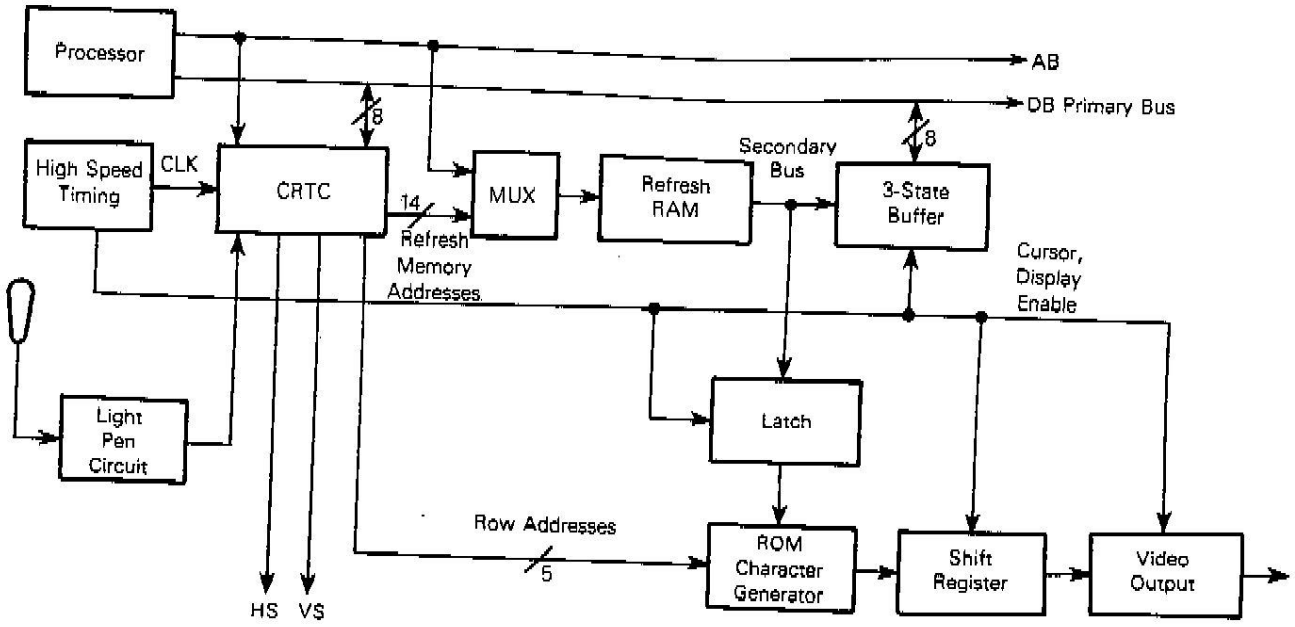
PIN ASSIGNMENT



ORDERING INFORMATION

Package Type	Frequency (MHz)	Temperature	Order Number
Ceramic L Suffix	1.0	0°C to 70°C	MC6845L
	1.0	−40°C to 85°C	MC6845CL
	1.5	0°C to 70°C	MC68A45L
	1.5	−40°C to 85°C	MC68A45CL
	2.0	0°C to 70°C	MC68B45L
Cerdip S Suffix	1.0	0°C to 70°C	MC6845S
	1.0	−40°C to 85°C	MC6845CS
	1.5	0°C to 70°C	MC68A45S
	1.5	−40°C to 85°C	MC68A45CS
	2.0	0°C to 70°C	MC68B45S
Plastic P Suffix	1.0	0°C to 70°C	MC6845P
	1.0	−40°C to 85°C	MC6845CP
	1.5	0°C to 70°C	MC68A45P
	1.5	−40°C to 85°C	MC68A45CP
	2.0	0°C to 70°C	MC68B45P

FIGURE 1 — TYPICAL CRT CONTROLLER APPLICATION



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range MC6845, MC68A45, MC68B45 MC6845C, MC68A45C	T_A	T_L to T_H 0 to 70 −40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Rating
Thermal Resistance Plastic Package Cerdip Package Ceramic Package	θ_{JA}	 100 60 50	°C/W

The device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{CC}$.

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	−0.3	–	0.8	V
Input High Voltage	V_{IH}	2.0	–	V_{CC}	V

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Where:

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{PORT}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

P_{PORT} = Port Power Dissipation, Watts — User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted, see Figures 2-4)

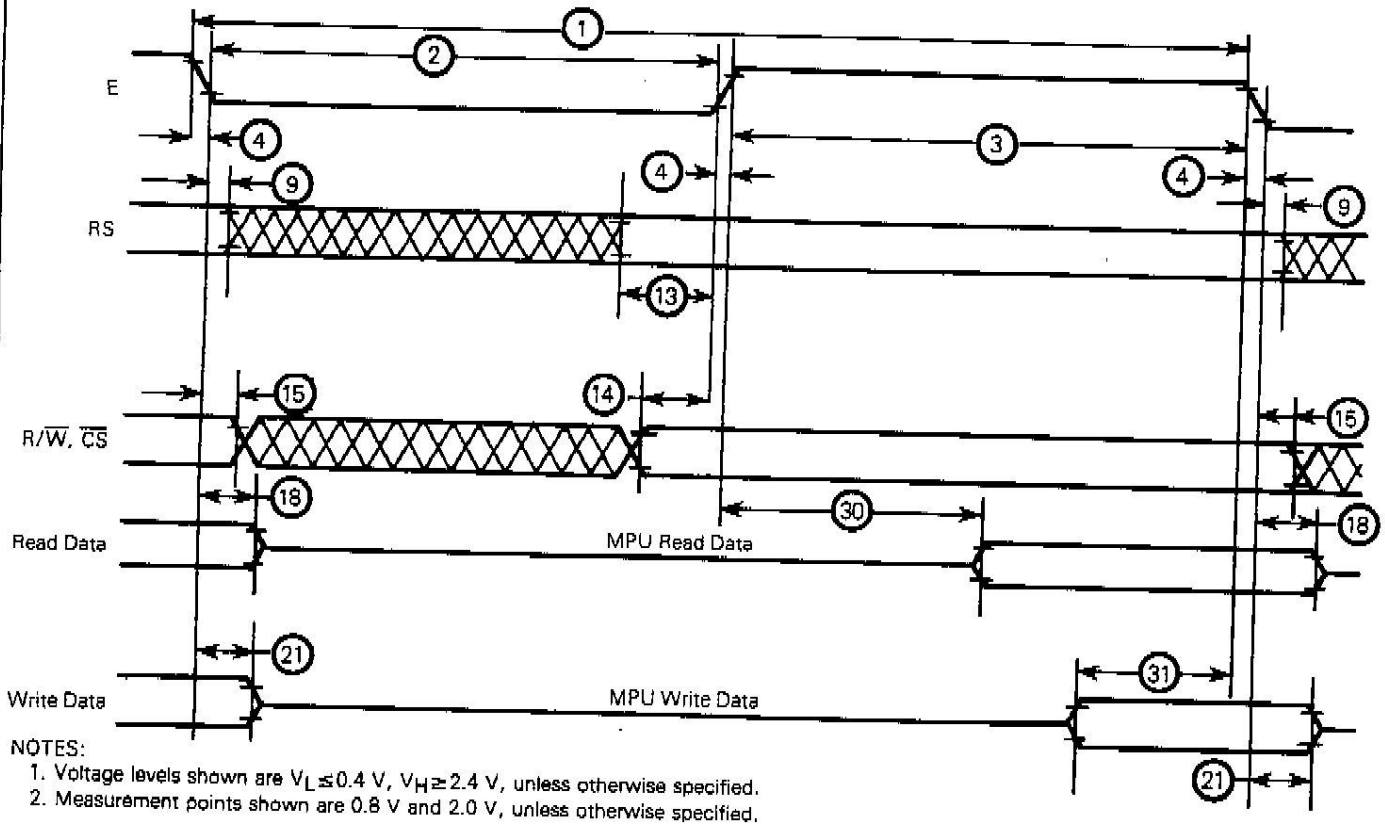
Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage		V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage		V_{IL}	−0.3	—	0.8	V
Input Leakage Current		I_{in}	—	0.1	2.5	μA
Hi-Z State Input Current (V_{CC} = 5.25 V) (V_{in} = 0.4 to 2.4 V)		I_{TSI}	−10	—	10	μA
Output High Voltage (I_{Load} = −205 μA) (I_{Load} = −100 μA)	D0-D7 Other Outputs	V_{OH}	2.4 2.4	3.0 3.0	— —	V
Output Low Voltage (I_{Load} = 1.6 mA)		V_{OL}	—	0.3	0.4	V
Internal Power Dissipation (Measured at T_A = 0°C)		P_{INT}	—	600	750	mW
Input Capacitance	D0-D7 All Others	C_{in}	— —	— —	12.5 10	pF
Output Capacitance	All Outputs	C_{out}	—	—	10	pF

BUS TIMING CHARACTERISTICS (See Notes 1 and 2) (Reference Figures 2 and 3)

Ident. Number	Characteristic	Symbol	MC6845		MC68A45		MC68B45		Unit
			Min	Max	Min	Max	Min	Max	
1	Cycle Time	t_{cyc}	1.0	10**	0.67	10	0.5	10**	μs
2	Pulse Width, E Low	PW_{EL}	430	–	280	–	210	–	ns
3	Pulse Width, E High	PW_{EH}	450	–	280	–	220	–	ns
4	Clock Rise and Fall Time	t_r, t_f	–	25	–	25	–	20	ns
9	Address Hold Time (RS)	t_{AH}	10	–	10	–	10	–	ns
13	RS Setup Time Before E	t_{AS}	80	–	60	–	40	–	ns
14	R/$\overline{W}$ and $\overline{CS}$ Setup Time Before E	t_{CS}	80	–	60	–	40	–	ns
15	R/$\overline{W}$ and $\overline{CS}$ Hold Time	t_{CH}	10	–	10	–	10	–	ns
18	Read Data Hold Time	t_{DHR}	20	50*	20	50*	20	50*	ns
21	Write Data Hold Time	t_{DHW}	10	–	10	–	10	–	ns
30	Peripheral Output Data Delay Time	t_{DDR}	–	290	–	180	0	150	ns
31	Peripheral Input Data Setup Time	t_{DSW}	165	–	80	–	60	–	ns

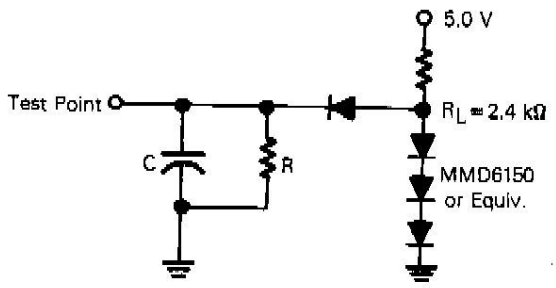
*The data bus output buffers are no longer sourcing or sinking current by t_{DHR} maximum (high impedance).
**The E clock may be low for extended periods provided the CLK input is active.

FIGURE 2 — MC6845 BUS TIMING



NOTES:
1. Voltage levels shown are $V_L \leq 0.4$ V, $V_H \geq 2.4$ V, unless otherwise specified.
2. Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.

FIGURE 3 — BUS TIMING TEST LOAD



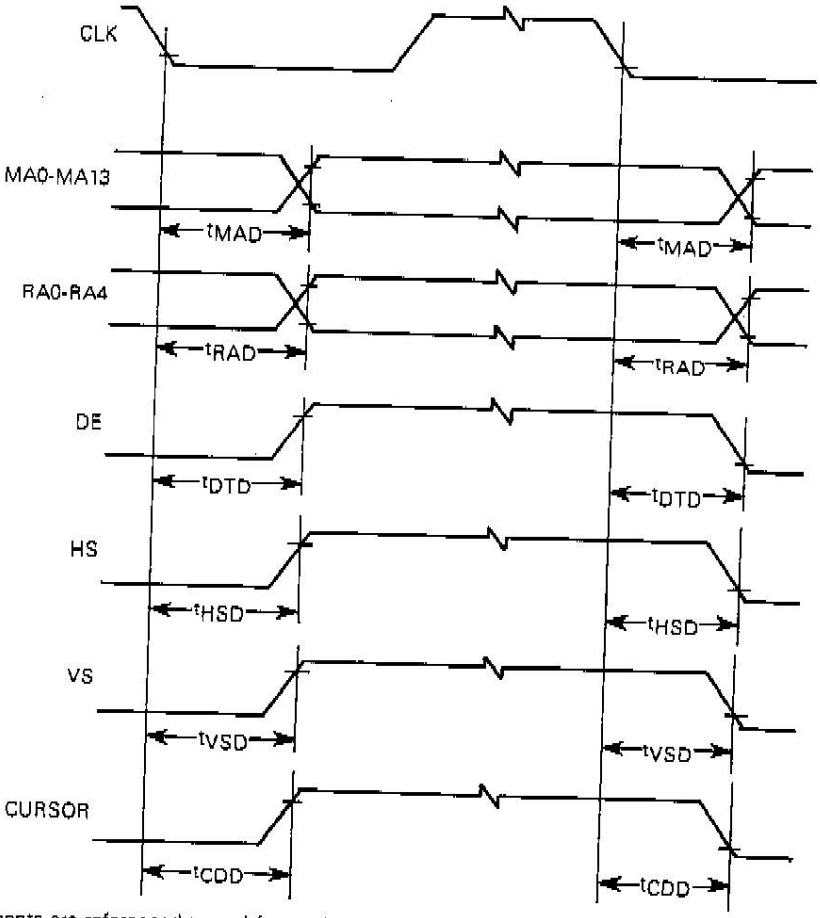
C = 130 pF for D0-D7
= 30 pF for MA0-MA13, RA0-RA4, DE, HS, VS, and CURSOR
R = 11 kΩ for D0-D7
= 24 kΩ for All Other Outputs

CRTC TIMING CHARACTERISTICS (Reference Figures 4 and 5)

Characteristic	Symbol	Min	Max	Unit
Minimum Clock Pulse Width, Low	P_{WCL}	150	–	ns
Minimum Clock Pulse Width, High	P_{WCH}	150	–	ns
Clock Frequency	f_c	–	3.0	MHz
Rise and Fall Time for Clock Input	t_{cr}, t_{cf}	–	20	ns
Memory Address Delay Time	t_{MAD}	–	160	ns
Raster Address Delay Time	t_{RAD}	–	160	ns
Display Timing Delay Time	t_{DTD}	–	250	ns
Horizontal Sync Delay Time	t_{HSD}	–	250	ns
Vertical Sync Delay Time	t_{VSD}	–	250	ns
Cursor Display Timing Delay Time	t_{CDD}	–	250	ns
Light Pen Strobe Minimum Pulse Width	PW_{LPH}	80	–	ns
Light Pen Strobe Disable Time	t_{LPD1}	–	80	ns
	t_{LPD2}	–	10	ns

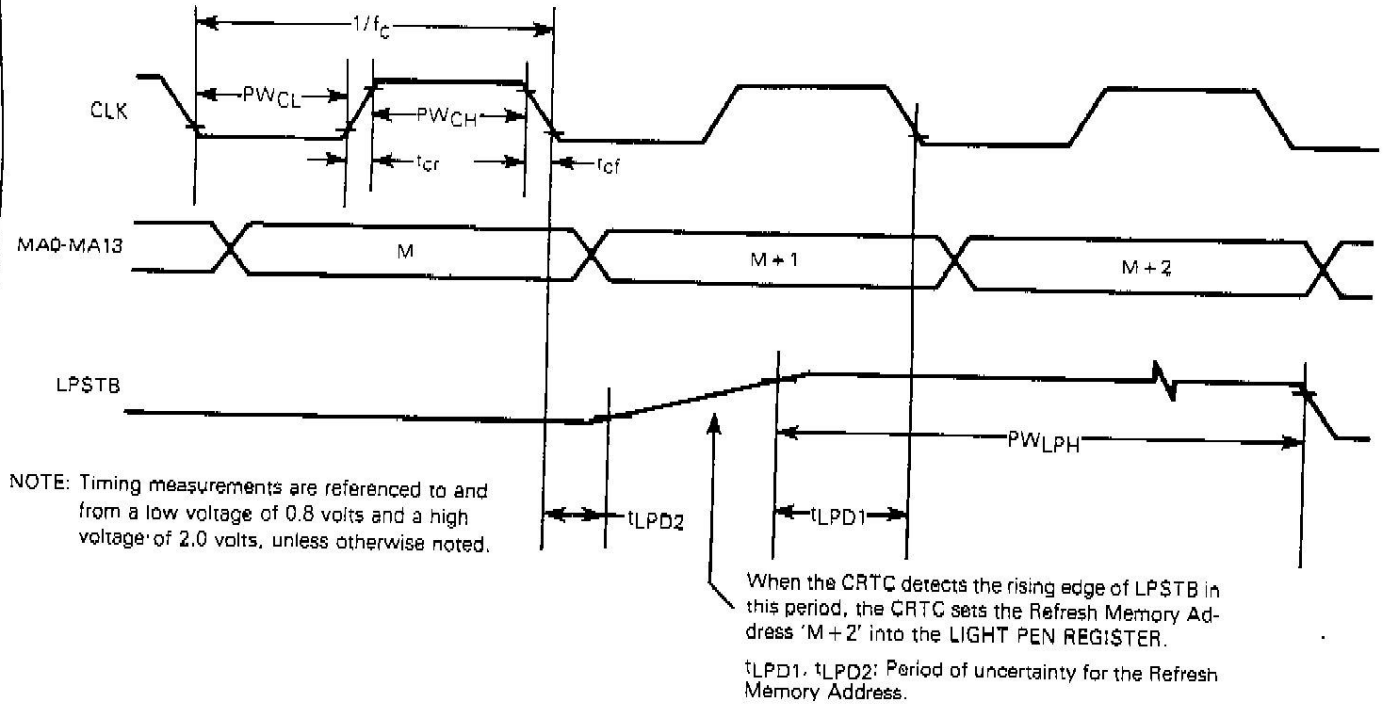
NOTE: The light pen strobe must fall to low level before VS pulse rises.

FIGURE 4 – CRTC TIMING CHART



NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts unless otherwise noted.

FIGURE 5 — CRTC-CLK, MA0-MA13, AND LPSTB TIMING DIAGRAM



NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

t_{LPD1}, t_{LPD2}: Period of uncertainty for the Refresh Memory Address.

CRTC INTERFACE SYSTEM DESCRIPTION

The CRT controller generates the signals necessary to interface a digital system to a raster scan CRT display. In this type of display, an electron beam starts in the upper left hand corner, moves quickly across the screen and returns. This action is called a horizontal scan. After each horizontal scan the beam is incrementally moved down in the vertical direction until it has reached the bottom. At this point one frame has been displayed, as the beam has made many horizontal scans and one vertical scan.

Two types of raster scanning are used in CRTs, interlace and non-interlace, shown in Figures 6 and 7. Non-interlace scanning consists of one field per frame. The scan lines in Figure 6 are shown as solid lines and the retrace patterns are indicated by the dotted lines. Increasing the number of frames per second will decrease the flicker. Ordinarily, either a 50 or 60 frame per second refresh rate is used to minimize beating between the CRT and the power line frequency. This prevents the displayed data from weaving.

Interlace scanning is used in broadcast TV and on data monitors where high density or high resolution data must be displayed. Two fields, or vertical scans are made down the screen for each single picture or frame. The first field (even field) starts in the upper left hand corner; the second (odd field) in the upper center. Both fields overlap as shown in Figure 7, thus interlacing the two fields into a single frame.

In order to display the characters on the CRT screen the frames must be continually repeated. The data to be displayed is stored in the refresh (screen) memory by the MPU controlling the data processing system. The data is usually written in ASCII code, so it cannot be directly displayed as characters. A character generator ROM is typically used to convert the ASCII codes into the "dot" pattern for every character.

The most common method of generating characters is to create a matrix of dots "x" dots (columns) wide and "y" dots (rows) high. Each character is created by selectively filling in

FIGURE 6 — RASTER SCAN SYSTEM (NON-INTERLACE)

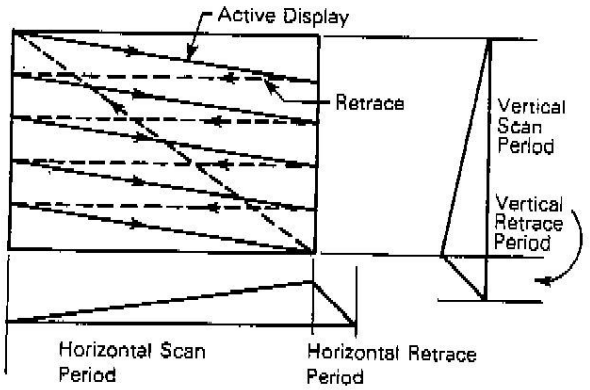
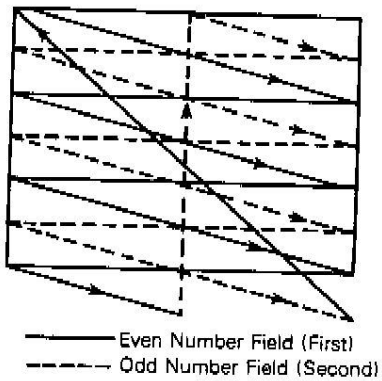


FIGURE 7 — RASTER SCAN SYSTEM (INTERLACE)



the dots. As "x" and "y" get larger a more detailed character may be created. Two common dot matrices are 5 x 7 and 7 x 9. Many variations of these standards will allow Chinese, Japanese, or Arabic letters instead of English. Since characters require some space between them, a character block larger than the character is typically used, as shown in Figure 8. The figure also shows the corresponding timing and levels for a video signal that would generate the characters.

Referring to Figure 1, the CRT controller generates the refresh addresses (MA0-MA13), row addresses (RA0-RA4), and the video timing (vertical sync – VS, horizontal sync – HS, and display enable – DE). Other functions include an internal cursor register which generates a cursor output when its contents compare to the current refresh address. A light pen strobe input signal allows capture of the refresh address in an internal light pen register.

All timing in the CRTC is derived from the CLK input. In alphanumeric terminals, this signal is the character rate. The video rate or "dot" clock is externally divided by high-speed logic (TTL) to generate the CLK input. The high-speed logic must also generate the timing and control signals necessary for the shift register, latch, and MUX control.

The processor communicates with the CRTC through an 8-bit data bus by reading or writing into the 19 registers.

The refresh memory address is multiplexed between the processor and the CRTC. Data appears on a secondary bus separate from the processor's bus. The secondary data bus concept in no way precludes using the refresh RAM for other purposes. It looks like any other RAM to the processor. A number of approaches are possible for solving contentions for the refresh memory:

1. Processor always gets priority. (Generally, "hash" occurs as MPU and CRTC clocks are not synchronized.)
2. Processor gets priority access anytime, but can be synchronized by an interrupt to perform accesses only during horizontal and vertical retrace times.
3. Synchronize the processor with memory wait cycles (states).
4. Synchronize the processor to the character rate as shown in Figure 9. The M6800 processor family works works very well in this configuration as constant cycle lengths are present. This method provides no overhead for the processor as there is never a contention for a memory access. All accesses are transparent.

FIGURE 8 – CHARACTER DISPLAY ON THE SCREEN AND VIDEO SIGNAL

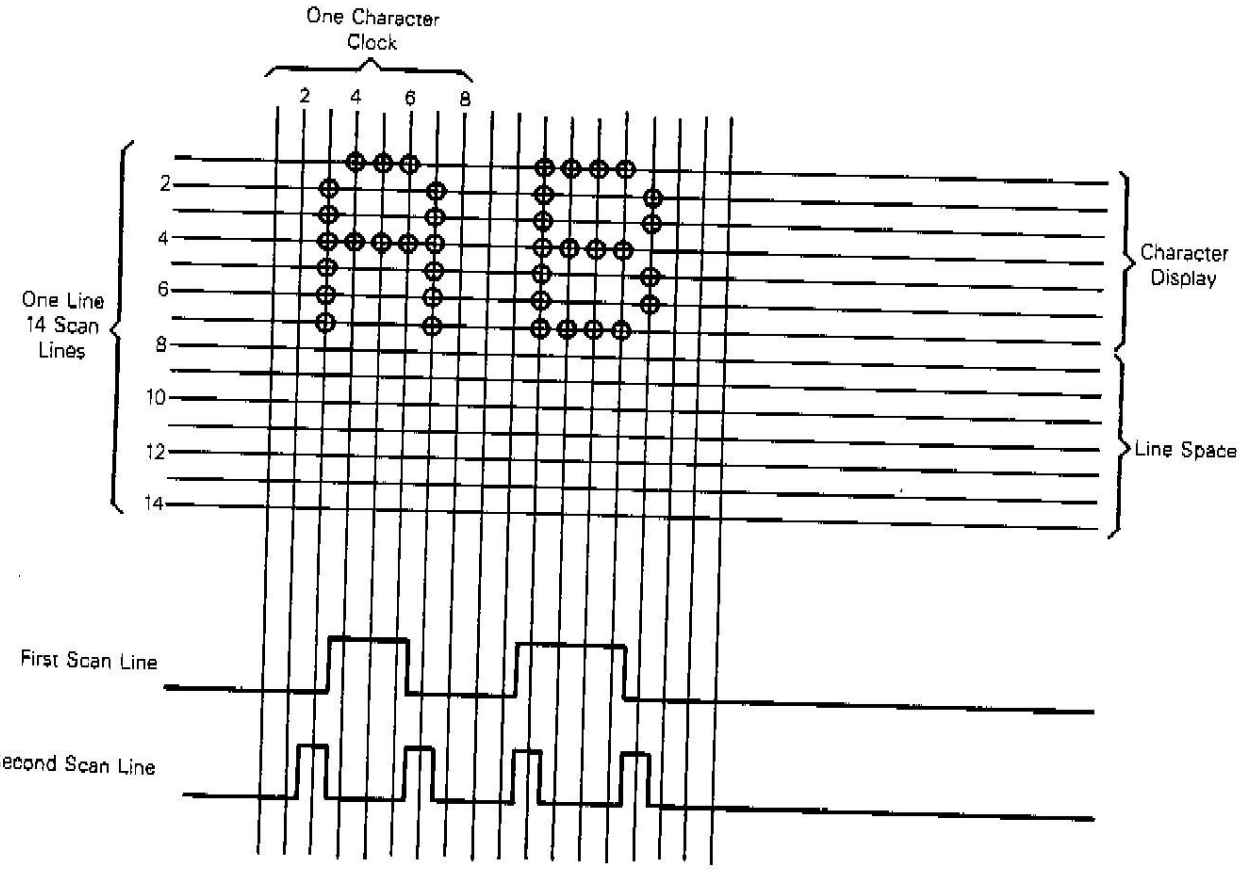
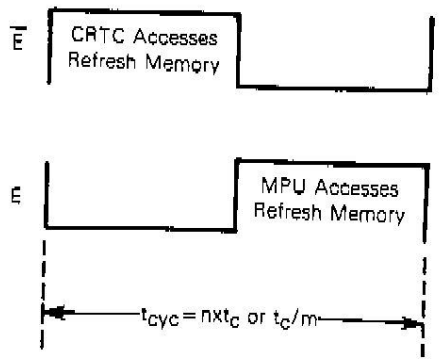


FIGURE 9 — TRANSPARENT REFRESH MEMORY CONFIGURATION TIMING USING M6800 FAMILY MPU



Where: m, n are integers; t_c is character period

PIN DESCRIPTION

PROCESSOR INTERFACE

The CRTC interfaces to a processor bus on the bidirectional data bus (D0-D7) using $\overline{CS}$, RS, E, and R/$\overline{W}$ for control signals.

Data Bus (D0-D7) — The bidirectional data lines (D0-D7) allow data transfers between the internal CRTC register file and the processor. Data bus output drivers are in the high-impedance state until the processor performs a CRTC read operation.

Enable (E) — The enable signal is a high-impedance TTL/MOS compatible input which enables the data bus input/output buffers and clocks data to and from the CRTC. This signal is usually derived from the processor clock. The high-to-low transition is the active edge.

Chip Select ($\overline{CS}$) — The $\overline{CS}$ line is a high-impedance TTL/MOS compatible input which selects the CRTC, when low, to read or write to the internal register file. This signal should only be active when there is a valid stable address being decoded from the processor.

Register Select (RS) — The RS line is a high-impedance TTL/MOS compatible input which selects either the address register (RS = 0) or one of the data register (RS = 1) or the internal register file.

Read/Write (R/$\overline{W}$) — The R/$\overline{W}$ line is a high-impedance TTL/MOS compatible input which determines whether the internal register file gets written or read. A write is defined as a low level.

CRT CONTROL

The CRTC provides horizontal sync (HS), vertical sync (VS), and display enable (DE) signals.

NOTE

Care should be exercised when interfacing to CRT monitors, as many monitors claiming to be "TTL compatible" have transistor input circuits which require the CRTC or TTL devices buffering signals from the CRTC/video circuits to exceed the maximum-rated drive currents.

Vertical Sync (VS) and Horizontal Sync (HS) — These TTL-compatible outputs are active high signals which drive the monitor directly or are fed to the video processing circuitry to generate a composite video signal. The VS signal determines the vertical position of the displayed text while the HS signal determines the horizontal position of the displayed text.

Display Enable (DE) — This TTL-compatible output is an active high signal which indicates the CRTC is providing addressing in the active display area.

REFRESH MEMORY/CHARACTER GENERATOR ADDRESSING

The CRTC provides memory addresses (MA0-MA13) to scan the refresh RAM. Row addresses (RA0-RA4) are also provided for use with character generator ROMs. In a graphics system, both the memory addresses and the row addresses would be used to scan the refresh RAM. Both the memory addresses and the row addresses continue to run during vertical retrace thus allowing the CRTC to provide the refresh addresses required to refresh dynamic RAMs.

Refresh Memory Addresses (MA0-MA13) — These 14 outputs are used to refresh the CRT screen with pages of data located within a 16K block of refresh memory. These outputs are capable of driving one standard TTL load and 30 pF.

Row Addresses (RA0-RA4) — These five outputs from the internal row address counter are used to address the character generator ROM. These outputs are capable of driving one standard TTL load and 30 pF.

OTHER PINS

Cursor — This TTL-compatible output indicates a valid cursor address to external video processing logic. It is an active high signal.

Clock (CLK) — The CLK is a TTL/MOS-compatible input used to synchronize all CRT functions except for the processor interface. An external dot counter is used to derive this signal which is usually the character rate in an alphanumeric CRT. The active transition is high-to-low.

Light Pen Strobe (LPSTB) — A low-to-high transition on this high-impedance TTL/MOS-compatible input latches the current Refresh Address in the light pen register. The latching of the refresh address is internally synchronized to the character clock (CLK).

V_{CC} and V_{SS} — These inputs supply +5 Vdc ±5% to the CRTC.

$\overline{RESET}$ — The $\overline{RESET}$ input is used to reset the CRTC. A low level on the $\overline{RESET}$ input forces the CRTC into the following state:

(a) All counters in the CRTC are cleared and the device stops the display operation.

(b) All the outputs are driven low.

NOTE

The horizontal sync output is not defined until after R2 is programmed.

(c) The control registers of the CRTC are not affected and remain unchanged.

Functionality of $\overline{RESET}$ differs from that of other M6800 parts in the following functions:

(a) The $\overline{RESET}$ input and the LPSTB input are encoded as shown in Table 1.

TABLE 1 — CRTC OPERATING MODE

$\overline{RESET}$	LPSTB	Operating Mode
0	0	Reset
0	1	Test Mode
1	0	Normal Mode
1	1	Normal Mode

The test mode configures the memory addresses as two independent 7-bit counters to minimize test time.

(b) After $\overline{RESET}$ has gone low and (LPSTB=0), MA0-MA13 and RA0-RA4 will be driven low on the falling edge of CLK. $\overline{RESET}$ must remain low for at least one cycle of the character clock (CLK).

(c) The CRTC resumes the display operation immediately after the release of $\overline{RESET}$. DE and the CURSOR are not active until after the first frame has been displayed.

CRTC DESCRIPTION

The CRTC consists of programmable horizontal and vertical timing generators, programmable linear address register, programmable cursor logic, light pen capture register, and control circuitry for interface to a processor bus. A block diagram of the CRTC is shown in Figure 10.

All CRTC timing is derived from the CLK, usually the output of an external dot rate counter. Coincidence (CO) circuits continuously compare counter contents to the contents of the programmable register file, R0-R17. For horizontal timing generation, comparisons result in: 1) horizontal sync pulse (HS) of a frequency, position, and width determined by the registers; 2) horizontal display signal of a frequency, position, and duration determined by the registers.

The horizontal counter produces H clock which drives the scan line counter and vertical control. The contents of the raster counter are continuously compared to the maximum scan line address register. A coincidence resets the raster counter and clocks the vertical counter.

Comparisons of vertical counter contents and vertical registers result in: 1) vertical sync pulse (VS) of a frequency and position determined by the registers; 2) vertical display of a frequency and position determined by the registers.

The vertical control logic has other functions.

1. Generate row selects, RA0-RA4, from the raster count for the corresponding interlace or non-interlace modes.
2. Extend the number of scan lines in the vertical total by the amount programmed in the vertical total adjust register.

The linear address generator is driven by the CLK and locates the relative positions of characters in memory with their positions on the screen. Fourteen lines, MA0-MA13, are available for addressing up to four pages of 4K characters, eight pages of 2K characters, etc. Using the start address register, hardware scrolling through 16K characters is possible. The linear address generator repeats the same sequence of addresses for each scan line of a character row.

The cursor logic determines the cursor location, size, and blink rate on the screen. All are programmable.

The light pen strobe going high causes the current contents of the address counter to be latched in the light pen register. The contents of the light pen register are subsequently read by the processor.

Internal CRTC registers are programmed by the processor through the data bus, D0-D7, and the control signals — R/$\overline{W}$, $\overline{CS}$, RS, and E.

REGISTER FILE DESCRIPTIONS

The nineteen registers of the CRTC may be accessed through the data bus. Only two memory locations are required as one location is used as a pointer to address one of the remaining eighteen registers. These eighteen registers control horizontal timing, vertical timing, interlace operation, row address operation, and define the cursor, cursor address, start address, and light pen register. The register addresses and sizes are shown in Table 2.

ADDRESS REGISTER

The address register is a 5-bit write-only register used as an "indirect"or "pointer" register. It contains the address of one of the other eighteen registers. When both RS and $\overline{CS}$ are low, the address register is selected. When $\overline{CS}$ is low and RS is high, the register pointed to by the address register is selected.

TIMING REGISTERS R0-R9

Figure 11 shows the visible display area of a typical CRT monitor giving the point of reference for horizontal registers as the left-most displayed character position. Horizontal registers are programmed in character clock time units with respect to the reference as shown in Figure 12. The point of reference for the vertical registers is the top character position displayed. Vertical registers are programmed in scan line times with respect to the reference as shown in Figure 13.

Horizontal Total Register (R0) — This 8-bit write-only register determines the horizontal sync (HS) frequency by defining the HS period in character times. It is the total of the displayed characters plus the non-displayed character times (retrace) minus one.

FIGURE 10 — CRTC BLOCK DIAGRAM

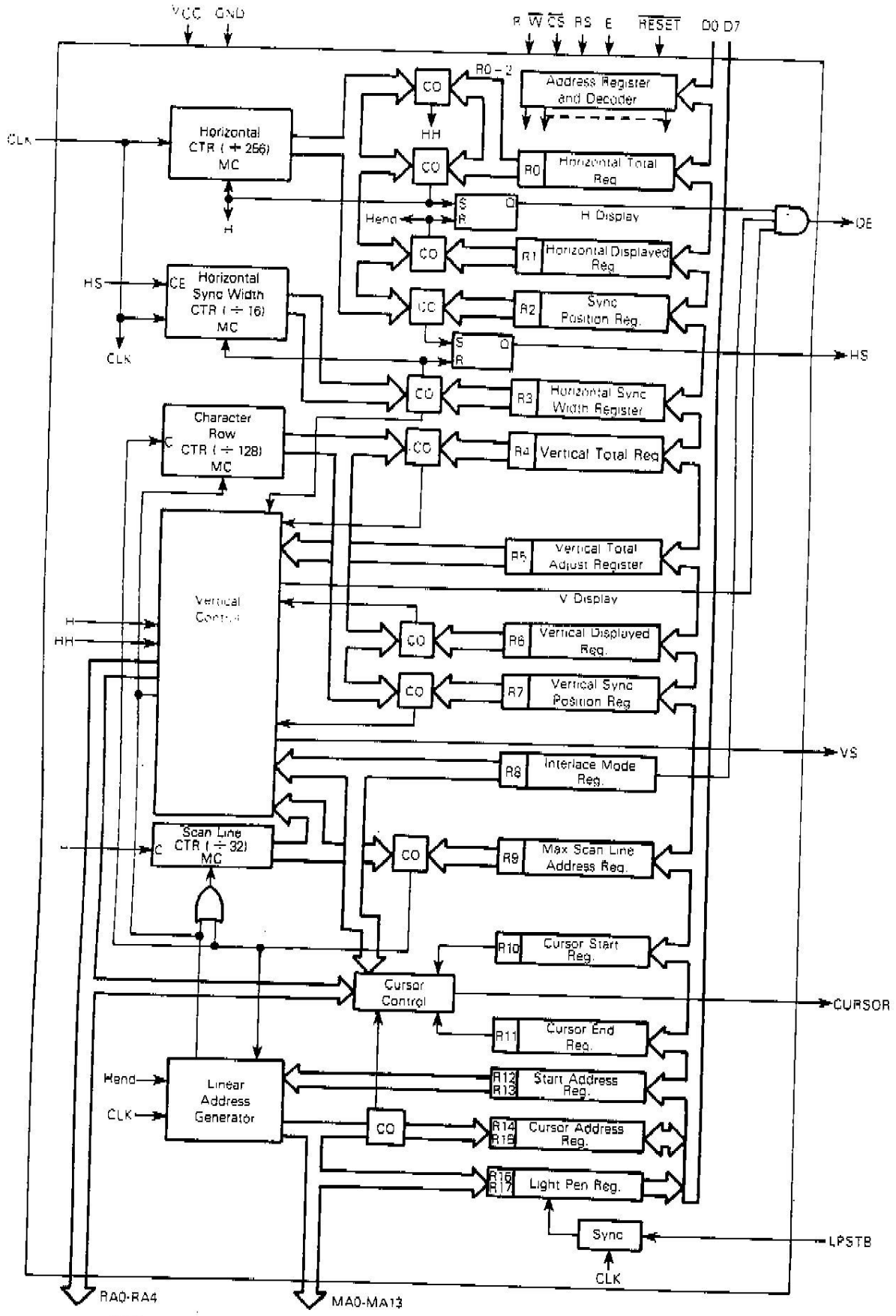
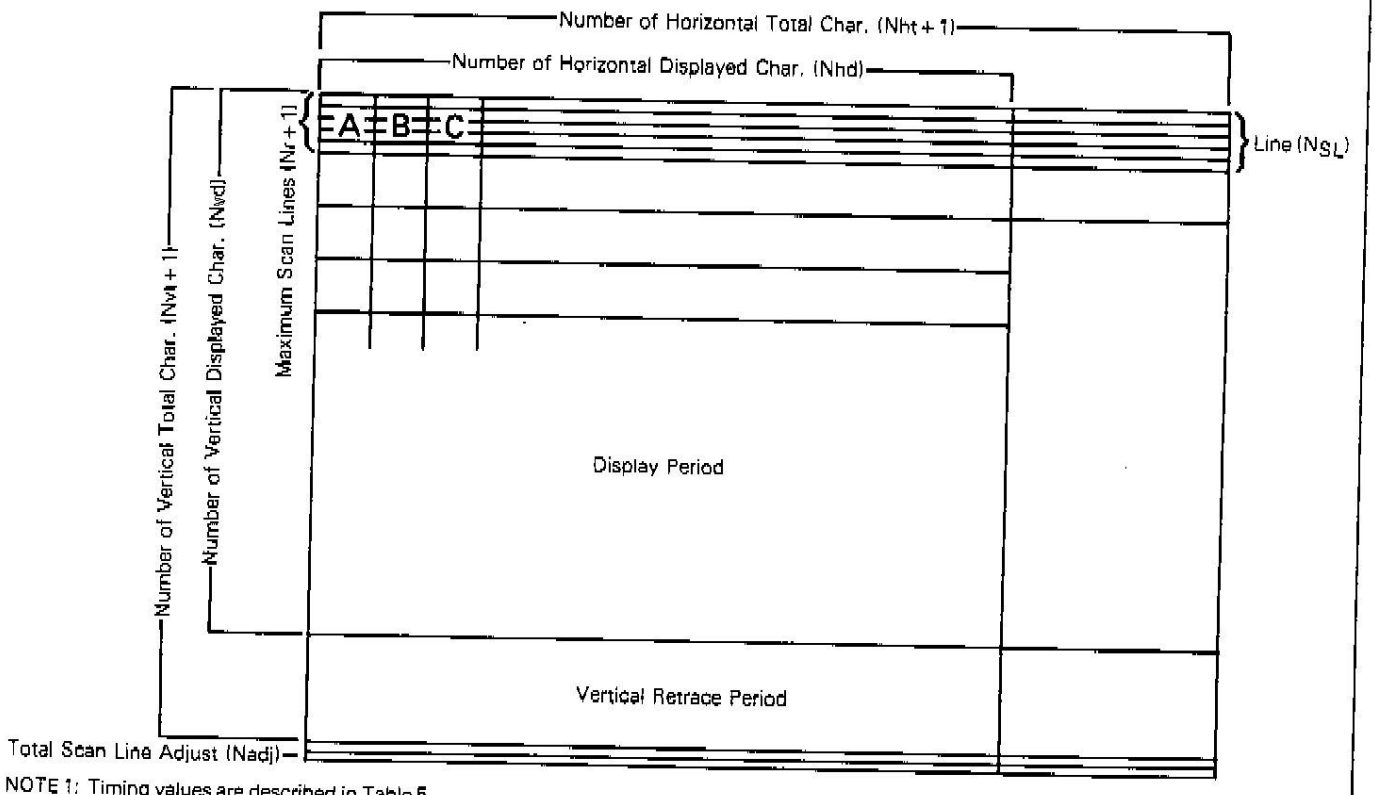


TABLE 2 – CRTC INTERNAL REGISTER ASSIGNMENT

$\overline{CS}$	RS	Address Register 4	3	2	1	0	Register #	Register File	Program Unit	Read	Write	Number of Bits 7	6	5	4	3	2	1	0
1	X	X	X	X	X	X	X	–	–	–	–	\	\	\	\	\	\	\	\
0	0	X	X	X	X	X	AR	Address Register	–	No	Yes	\	\	\					
0	1	0	0	0	0	0	R0	Horizontal Total	Char.	No	Yes								
0	1	0	0	0	0	1	R1	Horizontal Displayed	Char.	No	Yes								
0	1	0	0	0	1	0	R2	H. Sync Position	Char.	No	Yes								
0	1	0	0	0	1	1	R3	Sync Width	–	No	Yes	\	\	\	\	H	H	H	H
0	1	0	0	1	0	0	R4	Vertical Total	Char. Row	No	Yes	\							
0	1	0	0	1	0	1	R5	V. Total Adjust	Scan Line	No	Yes	\	\	\					
0	1	0	0	1	1	0	R6	Vertical Displayed	Char. Row	No	Yes	\							
0	1	0	0	1	1	1	R7	V. Sync Position	Char. Row	No	Yes	\							
0	1	0	1	0	0	0	R8	Interlace Mode and Skew	Note 1	No	Yes	\	\	\	\	\	\	I	I
0	1	0	1	0	0	1	R9	Max Scan Line Address	Scan Line	No	Yes	\	\	\					
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line	No	Yes	\	B	P			(Note 2)		
0	1	0	1	0	1	1	R11	Cursor End	Scan Line	No	Yes	\	\	\					
0	1	0	1	1	0	0	R12	Start Address (H)	–	No	Yes	0	0						
0	1	0	1	1	0	1	R13	Start Address (L)	–	No	Yes								
0	1	0	1	1	1	0	R14	Cursor (H)	–	Yes	Yes	0	0						
0	1	0	1	1	1	1	R15	Cursor (L)	–	Yes	Yes								
0	1	1	0	0	0	0	R16	Light Pen (H)	–	Yes	No	0	0						
0	1	1	0	0	0	1	R17	Light Pen (L)	–	Yes	No								

NOTES:
1. The interlace is shown in Table 3.
2. Bit 5 of the cursor start raster register is used for blink period control, and bit 6 is used to select blink or no-blink.

FIGURE 11 – ILLUSTRATION OF THE CRT SCREEN FORMAT



NOTE 1: Timing values are described in Table 5.

Horizontal Displayed Register (R1) — This 8-bit write-only register determines the number of displayed characters per line. Any 8-bit number may be programmed as long as the contents of R0 are greater than the contents of R1.

Horizontal Sync Position Register (R2) — This 8-bit write-only register controls the HS position. The horizontal sync position defines the horizontal sync delay (front porch) and the horizontal scan delay (back porch). When the programmed value of this register is increased, the display on the CRT screen is shifted to the left. When the programmed value is decreased the display is shifted to the right. Any 8-bit number may be programmed as long as the sum of the contents of R2 and R3 are less than the contents of R0. R2 must be greater than R1.

Sync Width Register (R3) — This 8-bit write-only register determines the width of the horizontal sync (HS) pulse. The vertical sync pulse width is fixed at 16 scan-line times.

The HS pulse width may be programmed from 1-to-15 character clock periods thus allowing compatibility with the HS pulse width specifications of many different monitors. If zero is written into this register then no HS is provided.

Horizontal Timing Summary (Figure 12) — The difference between R0 and R1 is the horizontal blanking interval. This interval in the horizontal scan period allows the beam to return (retrace) to the left side of the screen. The retrace time is determined by the monitor's horizontal scan components. Retrace time is less than the horizontal blanking interval. A good rule of thumb is to make the horizontal blanking about 20% of the total horizontal scanning period for a CRT. In inexpensive TV receivers, the beam overscans the display screen so that aging of parts does not result in underscanning. Because of this, the retrace time should be about one third the horizontal scanning period. The horizontal sync delay, HS pulse width, and horizontal scan delay are typically programmed with a 1:2:2 ratio.

Vertical Total Register (R4) and Vertical Total Adjust Register (R5) — The frequency of VS is determined by both R4 and R5. The calculated number of character row times is usually an integer plus a fraction to get exactly a 50 or 60 Hz vertical refresh rate. The integer number of character row times minus one is programmed in the 7-bit write-only vertical total register (R4). The fraction of character line times is programmed in the 5-bit write-only vertical total adjust register (R5) as the number of scan lines required.

Vertical Displayed Register (R6) — This 7-bit write-only register specifies the number of displayed character rows on the CRT screen, and is programmed in character row times. Any number smaller than the contents of R4 may be programmed into R6.

Vertical Sync Position (R7) — This 7-bit write-only register controls the position of vertical sync with respect to the reference. It is programmed in character row times. When the programmed value of this register is increased, the display position of the CRT screen is shifted up. When the programmed value is decreased the display position is shifted down. Any number equal to or less than the vertical total (R4) and greater than or equal to the vertical displayed (R6) may be used.

Interlace Mode and Skew Register (R8) — The MC6845 only allows control of the interlace modes as programmed by the low order two bits of this write-only register. Table 3 shows the interlace modes available to the user. These modes are selected using the two low order bits of this 6-bit write-only register.

TABLE 3 — INTERLACE MODE REGISTER

Bit 1	Bit 0	Mode
0	0	Normal Sync Mode (Non-Interlace)
1	0	
0	1	Interlace Sync Mode
1	1	Interlace Sync and Video Mode

In the normal sync mode (non-interlace) only one field is available as shown in Figures 6 and 14a. Each scan line is refreshed at the VS frequency (e.g., 50 or 60 Hz).

Two interlace modes are available as shown in Figures 7, 14b, and 14c. The frame time is divided between even and odd alternating fields. The horizontal and vertical timing relationship (VS delayed by one half scan line time) results in the displacement of scan lines in the odd field with respect to the even field.

In the interlace sync mode the same information is painted in both fields as shown in Figure 14b. This is a useful mode for filling in a character to enhance readability.

In the interlace sync and video mode, shown in Figure 14c, alternating lines of the character are displayed in the even field and the odd field. This effectively doubles the given bandwidth of the CRT monitor.

Care must be taken when using either interlace mode to avoid an apparent flicker effect. This flicker effect is due to the doubling of the refresh time for all scan lines since each field is displayed alternately and may be minimized with proper monitor design (e.g., longer persistence phosphors).

In addition, there are restrictions on the programming of the CRTC registers for interlace operation:

1. The horizontal total register value, R0, must be odd (i.e., an even number of character times).
2. For interlace sync and video mode only, the maximum scan-line address, R9, must be odd (i.e., an even number of scan lines).
3. For interlace sync and video mode only, the number (Nvd) programmed into the vertical display register (R6) must be one half the actual number required. The even numbered scan lines are displayed in the even field and the odd numbered scan lines are displayed in the odd field.
4. For interlace sync and video mode only, the cursor start register (R10) and cursor end register (R11) must both be even or both odd depending on which field the cursor is to be displayed in. A full block cursor will be displayed in both the even and the odd field when the cursor end register (R11) is programmed to a value greater than the value in the maximum scan line address register (R9).

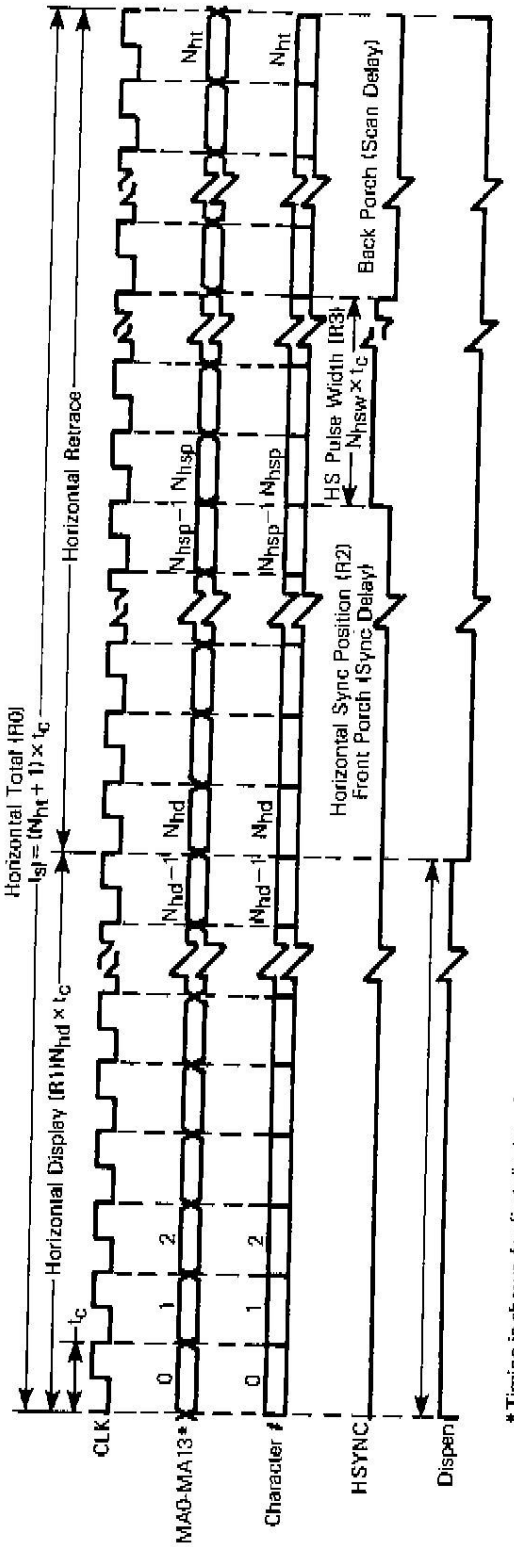
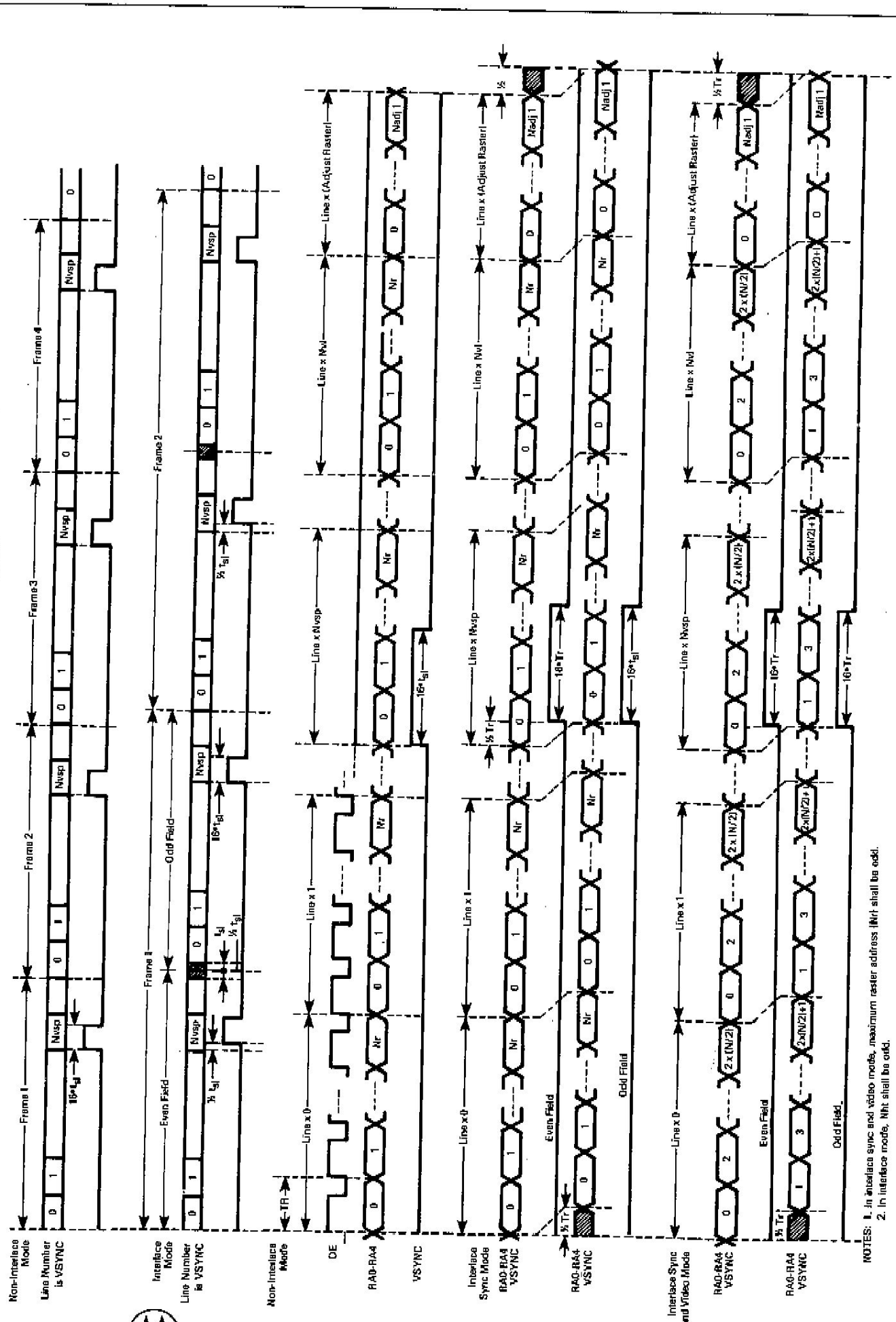


FIGURE 12 – CRTC HORIZONTAL TIMING

*Timing is shown for first displayed scan row only. See chart in Figure 15 for other rows. The initial MA is determined by the contents of start address register, R12/R13. Timing is shown for R12/R13 = 0.

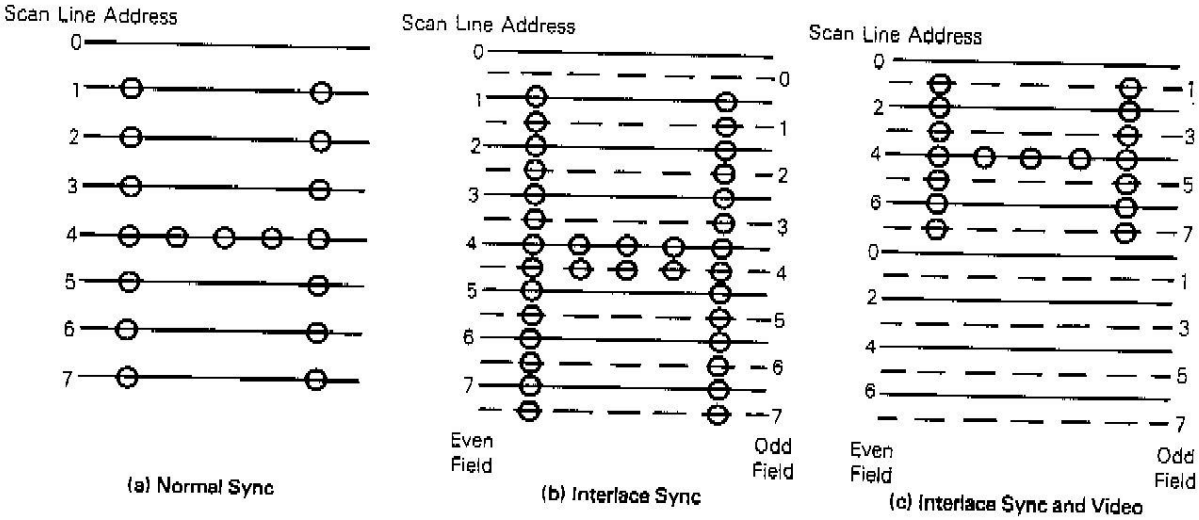
NOTE: Timing values are described in Table 5.

FIGURE 13 – CRTC VERTICAL TIMING



NOTES: 1. In interlace sync and video mode, maximum raster address (Nvtr) shall be odd.
2. In interlace mode, Nht shall be odd.

FIGURE 14 – INTERLACE CONTROL



Maximum Scan Line Address Register (R9) – This 5-bit write-only register determines the number of scan lines per character row including the spacing; thus, controlling operation of the row address counter. The programmed value is a maximum address and is one less than the number of scan lines.

CURSOR CONTROL

Cursor Start Register (R10) and Cursor End Reigster (R11) – These registers allow a cursor of up to 32 scan lines in height to be placed on any scan line of the character block as shown in Figure 15. R10 is a 7-bit write-only register used to define the start scan line and the cursor blink rate. Bits 5 and 6 of the cursor start address register control the cursor operation as shown in Table 4. Non-display, display, and two blink modes (16 times or 32 times the field period) are available. R11 is a 5-bit write-only register which defines the last scan line of the cursor.

TABLE 4 – CURSOR START REGISTER

Bit 6	Bit 5	Cursor Display Mode
0	0	Non-Blink
0	1	Cursor Non-Display
1	0	Blink, 1/16 Field Rate
1	1	Blink, 1/32 Field Rate

Example of cursor display mode

When an external blink feature on characters is required, it may be necessary to perform cursor blink externally so that both blink rates are synchronized. Note that an invert/non-invert cursor is easily implemented by programming the CRTC for a blinking cursor and externally inverting the video signal with an exclusive-OR gate.

Cursor Register (R14-H, R15-L) – This 14-bit read/write register pair is programmed to position the cursor anywhere in the refresh RAM area; thus, allowing hardware paging and scrolling through memory without loss of the original cursor position. It consists of an 8-bit low order (MA0-MA7) register and a 6-bit high order (MA8-MA13) register.

OTHER REGISTERS

Start Address Register (R12-H, R13-L) – This 14-bit write-only register pair controls the first address output by the CRTC after vertical blanking. It consists of an 8-bit low order (MA0-MA7) register and a 6-bit high order (MA8-MA13) register. The start address register determines which portion of the refresh RAM is displayed on the CRT screen. Hardware scrolling by character or page may be accomplished by modifying the contents of this register.

Light Pen Register (R16-H, R17-L) – This 14-bit read-only register pair captures the refresh address output by the CRTC on the positive edge of a pulse input to the LPSTB pin. It consists of an 8-bit low order (MA0-MA7) register and a 6-bit high order (MA8-MA13) register. Since the light pen pulse is asynchronous with respect to refresh address timing an internal synchronizer is designed into the CRTC. Due to delays (Figure 5) in this circuit, the value of R16 and R17 will need to be corrected in software. Figure 16 shows an interrupt driven approach although a polling routine could be used.

FIGURE 15 — CURSOR CONTROL

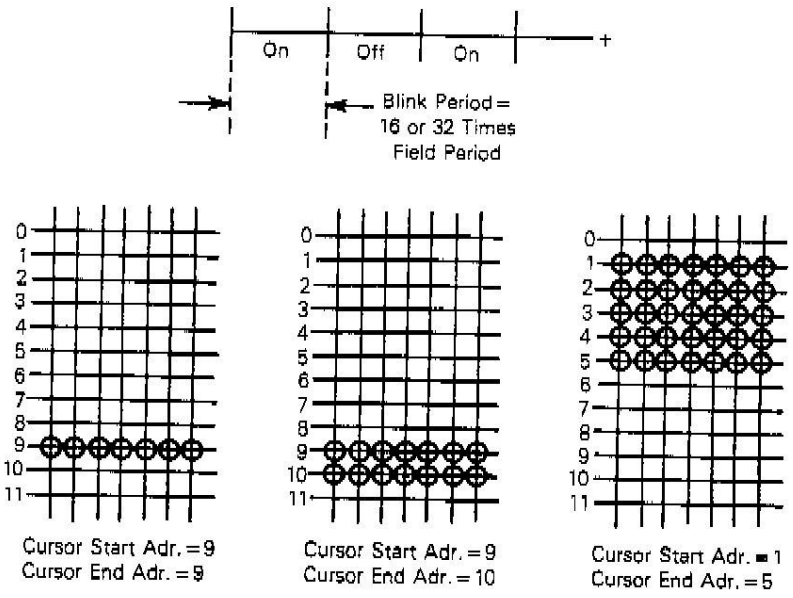
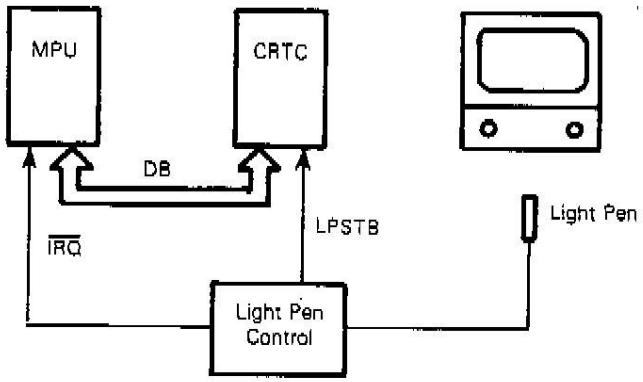


FIGURE 16 — INTERFACING OF LIGHT PEN



OPERATION OF THE CRTC

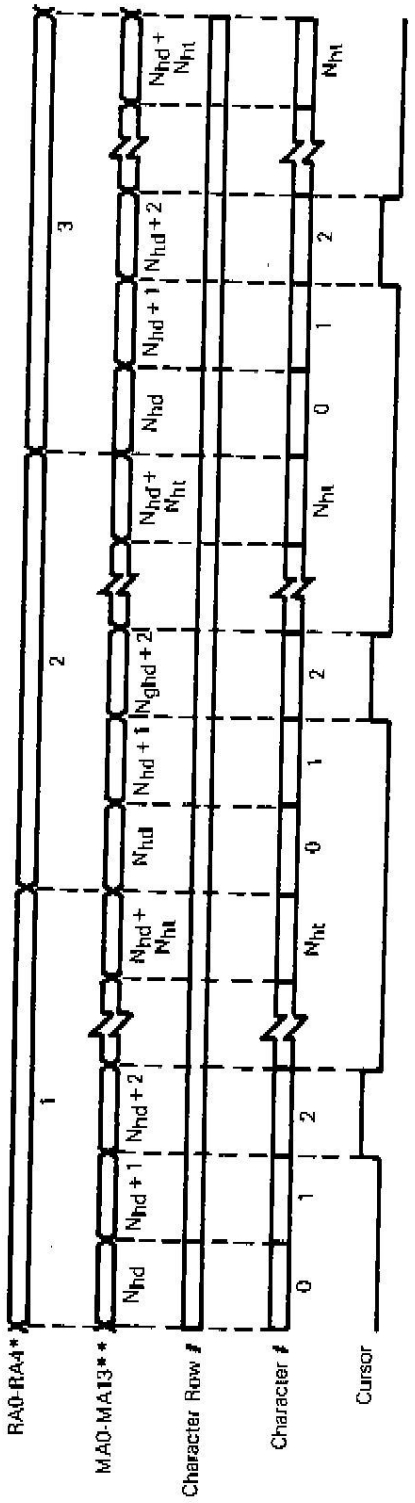
TIMING CHART OF THE CRT INTERFACE SIGNALS

Timing charts of CRT interface signals are illustrated in this section. When values listed in Table 5 are programmed into CRTC control registers, the device provides the outputs as shown in the timing diagrams (Figures 12, 13, 17, and 18). The screen format is shown in Figure 11 which illustrates the relation between refresh memory address (MA0-MA13), raster address (RA0-RA4), and the position on the screen. In this example, the start address is assumed to be zero.

TABLE 5 — VALUES PROGRAMMED INTO CRTC REGISTERS

Reg. #	Register Name	Value	Programmed Value
R0	H. Total	$N_{ht}+1$	N_{ht}
R1	H. Displayed	N_{hd}	N_{hd}
R2	H. Sync Position	N_{hsp}	N_{hsp}
R3	H. Sync Width	N_{hsw}	N_{hsw}
R4	V. Total	$N_{vt}+1$	N_{vt}
R5	V. Scan Line Adjust	N_{adj}	N_{adj}
R6	V. Displayed	N_{vd}	N_{vd}
R7	V. Sync Position	N_{vsp}	N_{vsp}
R8	Interlace Mode		
R9	Max. Scan Line Address	N_{sl}	N_{sl}

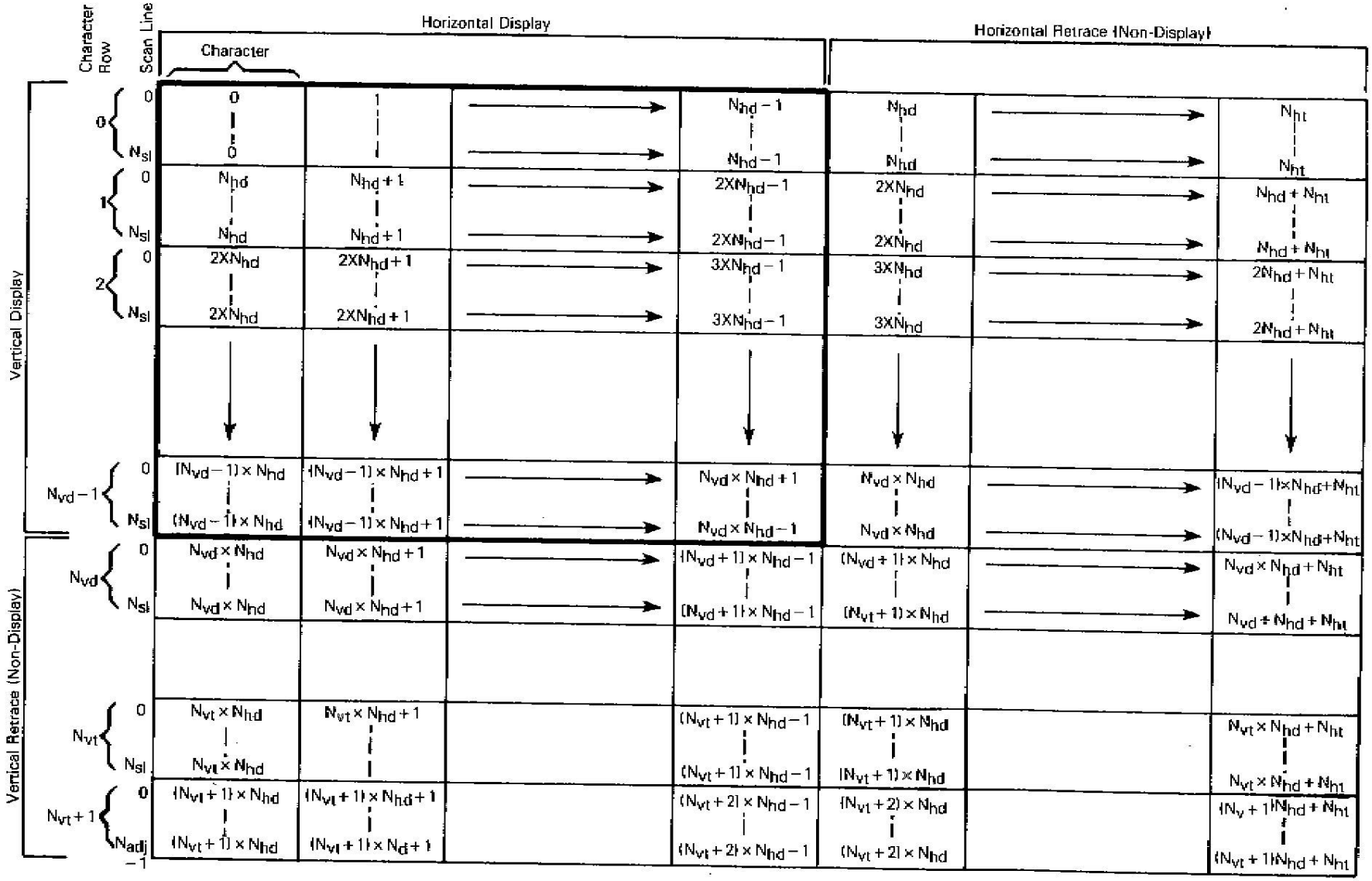
FIGURE 17 – CURSOR TIMING



*Timing is shown for non-interlace and interlace sync modes.
Example shown has cursor programmed as:
Cursor Register = $N_{hd}+2$
Cursor Start = 1
Cursor End = 3
**The initial MA is determined by the contents of start address register, R12/R13. Timing is shown for R12/R13=0.

NOTE 1: Timing values are described in Table 5.

FIGURE 18 — REFRESH MEMORY ADDRESSING (MA0-MA13) STAGE CHART



NOTE 1: The initial MA is determined by the contents of start address register, R12/R13. Timing is shown for R12/R13 = 0. Only non-interlace and interlace sync modes are shown.

DETERMINING REGISTER CONTENTS

Some of the register contents are determined rather easily. They are:

Register	Name	Contents
R8	Interlace Mode Register	See Table 3
R10	Cursor Start	See Figure 15 and Table 4
R11	Cursor End	See Figure 15
R12	Start Address (H)	User programs first memory location to be displayed
R13	Start Address (L)	
R14	Cursor (H)	User programs desired cursor location
R15	Cursor (L)	
R16	Light Pen (H)	Can be loaded via light-pen strobe only
R17	Light Pen (L)	

The remaining register contents must be determined from some basic data related to the CRT monitor and from the user-desired display format. The CRTC reference sheet (see Figure 19) gives a set of formulas for calculating the register contents as well as other useful characteristics of the display. This type of data is summarized under basic parameters in Figures 20 and 21; most or all of this data must be supplied by the user before he can determine the contents for registers R0-R7 and R9. All variables B_1-B_{10} are equal to basic parameters 1 through 10.

FIGURE 19 – CRTC REFERENCE SHEET

Register Function		Intermediate Calculations			Register Calculations	
R0	Horizontal Total	Symbol	Description	Calculation	Register	Calculation
R1	Horizontal Displayed	f'	Dot frequency (1st approx.)	$\frac{B_5 \cdot (B_7 + B_9)}{(1/B_1) - B_3}$	R0	$\frac{f'}{B_1 \cdot (B_7 + B_9)} - 1$
R2	Horizontal Sync Position					
R3	Horizontal Sync Width	t_c	Character Time	$\frac{1}{[(R0)+1] \cdot B_1}$	R1	B_5
R4	Vertical Total	f	Dot frequency	$\frac{B_7 + B_9}{t_c}$		
R5	Vertical Total Adjust				R2	$(R1) + \frac{(R3)}{2}$
R6	Vertical Displayed	t_{sl}	Scan line time	$[(R0)+1] \cdot t_c$	R3	$\frac{(R0) - (R1)}{3}$
R7	Vertical Sync Position	n	Total # of scan lines	$\frac{1}{B_2 \cdot t_{sl}}$		
R8	Interlace Mode				R4	$N - 1$
R9	Maximum Scan Line Address	N	Integer and	$\frac{n}{B_8 + B_{10}} = N + \frac{R}{B_8 + B_{10}}$	R5	R
R10	Cursor Start	R	Integer remainder			
R11	Cursor End				R6	B_6
R12	Start Address (H)	t_{cr}	Character row time	$(B_8 + B_{10}) \cdot t_{sl}$	R7	$[(R4)+1] - \frac{16 - (R5)}{B_8 + B_{10}} \geq (R7) \geq (R6)$
R13	Start Address (L)	t_{hr}	Horizontal retrace time	$\leq \frac{[(R0)+1-B_5] \cdot (B_7 + B_9)}{f}$		
R14	Cursor (H)				R9	$(B_8 + B_{10}) - 1$
R15	Cursor (L)	t_{vr}	Vertical retrace time	$\leq \frac{B1}{B2} - B_6 (B_8 + B_{10}) \cdot t_{sl}$		
R16	Light Pen (H)					
R17	Light Pen (L)					

In Figures 20 and 21, worksheet example calculations are shown for 32 × 16 and 80 × 24 display formats respectively. The following items are keyed to the figures. Basic parameters (1) through (10) have been provided; items (1) through (4) are data about the CRT monitor and items (5) through (10) are data about the user's desired display.

(1) Calculate the approximate dot frequency. The user should verify that the bandwidth of his CRT monitor will accomodate this frequency.
(2) Calculate R0. The resultant answer will usually be an integer plus a fraction. Assume the next high integer.
(3) Fill in value for R1.
(4) Calculate R3. Use the next highest integer. In these examples the sync width was chosen to be one third of the horizontal blanking interval.
(5) Calculate R2. Again, use the next highest integer.
(6) Calculate t_c, character tie. This is the time required for one scan line of one character block to be written.
(7) Calculate the exact dot frequency.
(8) Calculate t_{sl}, scan line time. This is the time required for one scan line of one character row to be written including retrace time.
(9) Calculate n. This is the total number of scan lines for each frame. Discard any fraction.
(10) Calculate N and R.
(11) Calculate R4.
(12) Fill in R5.
(13) Fill in R6.
(14) Calculate R7. If there is no possible value for R7, then the display demands for the CRT monitor exceed its capability. A compromise adjustment must be made in basic parameter 6, 8, or 10.
(15) Calculate R9.
(16) Calculate t_{cr}. This the time required for one character row to be written.
(17) Calculate t_{hr}. $t_{hr} > B_3$.
(18) Calculate t_{vr}. $t_{vr} > B_4$.

In Figure 20, calculation (B) verifies that the vertical period is 16.667 milliseconds or 60 hertz. The expression used is:

$$t_{cr} \times [(R4) + 1] + [t_{sl} \times (R5)] = V_P.$$

Another check is calculation of horizontal sync pulse width R3. $t_c = PW_{HS}$ (typically approximately equals 4 microseconds).

For convenience, a blank worksheet is provided in Figure 22.

FIGURE 20 — CRTC WORKSHEET EXAMPLE CALCULATION (32 × 16)

Basic Parameters (B1-B10)		Symbol	Intermediate Calculations		Value	Register		Decimal	Hex
1. Horizontal frequency	= 15750 ÷ 500	(1) f'	$\frac{32 \times (5+2)}{\frac{1}{15750} - 11 \times 10^{-6}}$	=	4.27×10^6	(2) R0	$\frac{4.27 \times 10^6}{15{,}750 \times (5+2)} - 1 =$	38	26
2. Vertical frequency	= 60	(6) t_c	$\frac{1}{39 \times 15750}$	=	1.63×10^{-6}	(3) R1	$B_5 = 32$	32	20
3. Minimum Horizontal retrace time	= 11×10^{-6}	(7) f	$\frac{5+2}{1.63 \times 10^{-6}}$	=	4.29×10^6	(5) R2	$\frac{32+3}{2}$	33	21
4. Minimum vertical retrace time	= 10^{-3}	(8) t_{sl}	$39 \times 1.63 \times 10^{-6}$	=	63.6×10^{-6}	(4) R3	$\frac{38-32}{3} =$	2	2
5. # of displayed characters per row	= 32	(9) n	$\frac{1}{60 \times 63.6 \times 10^{-6}}$	=	262	(11) R4	17 − 1 =	16	10
						(12) R5	R = 7	7	7
6. # of displayed charactor rows	= 16	(10) N			17	(13) R6	$B_6 = 16$	16	10
						(14) R7	(A)	16	10
7. # of dots in character dot matrix row	= 5	R	$\frac{262}{7+8}$	=	7	R8			
8. # of scan lines in charactor • matrix column	= 7	(16) t_{cr}	$(7+8) \times 63.6 \times 10^{-6}$	=	954×10^{-6}	(15) R9	7 + 8 − 1 =	14	0E
						R10			
9. Number of dots between horizontal adjacents	= 2	(17) t_{hr}	$\frac{(38+1-32) \bullet (5+2)}{4.29 \times 10^6}$	=	11.42×10^{-6}	R11			
10. Number of scan lines between vertical adjacents	= 8	(18) t_{vr}	$\left[\frac{15750}{60} - 16(7+8)\right] \times 63.6 \times 10^{-6}$	=	1.431×10^{-3}	R12			
						R13			
(A) $16 + 1 - \frac{16-7}{7+8} \geq (R7) \geq 16$ $17 - .6 \geq (R7) \geq 16$			(B) $954 \times 10^{-6} \times 17 = 16.218 \times 10^{-3}$ $+ \frac{63.6 \times 10^{-6} \times 7 = .445 \times 10^{-3}}{16.663 \text{ ms}} = \frac{1}{f}$ $f = 60$ Hz			R14			
						R15			

FIGURE 21 — CRTC WORKSHEET EXAMPLE CALCULATION (80 × 24)

Basic Parameters (B1-B10)		Symbol	Intermediate Calculations	Value	Register	Register Calculations	Decimal	Hex
1. Horizontal frequency	= 18,600	① f	$\frac{80 \cdot (7+2)}{\uparrow} - 11 \times 10^{-6}$ $\frac{}{18600}$	$16 \cdot 836 \times 10^{6}$	② R0	$\frac{16.836 \times 10^{6}}{(18,600)(9)} - 1$	100	64
2. Vertical frequency	= 60	⑥ t_c	$\frac{1}{(100+1) \cdot 18600}$	532.31×10^{-9}	③ R1	B5 = 80	80	50
					⑤ R2	$80 + \frac{7}{2}$	84	54
3. Minimum Horizontal retrace time	= 11×10^{-6}	⑦ f	$\frac{7+2}{532.31 \times 10^{-9}}$	16.907×10^{6}	④ R3	$\frac{R0 - R1}{3}$	7	07
4. Minimum vertical retrace time	= 1×10^{-3}	⑧ t_{sl}	$(100+1)(532.31 \times 10^{-9})$	53.76×10^{-6}	⑪ R4	28 − 1	27	1B
5. # of displayed characters per row	= 80	⑨ n	$\frac{1}{(60)(53.76 \times 10^{-6})}$	310	⑫ R5	R = 2	02	02
					⑬ R6	B6 = 24	24	18
6. # of displayed charactor rows	= 24	⑩ N		28	⑭ R7	Ⓐ	25	19
7. # of dots in character dot matrix row	= 7	R	$\frac{310}{11}$	2	R8		0	0
8. # of scan lines in charactor • matrix column	= 9	⑯ t_{cr}	$(9+2)(53.76 \times 10^{-6})$	591.39×10^{-6}	⑮ R9	(9+2) − 1	10	0A
					R10		00	00
9. Number of dots between horizontal adjacents	= 2	⑰ t_{hr}	$\leq \frac{(101-80)(7+2)}{16.907 \times 10^{6}}$	11.17×10^{-6}	R11		11	0B
					R12			00
10. Number of scan lines between vertical adjacents	= 2	⑱ t_{vr}	$\leq \left[\frac{18600}{60} - 24(11)\right] 53.76 \times 10^{-6}$	2.47×10^{-3}	R13		128	80
					R14		128	00
					R15			80

Ⓐ $(27+1) - \frac{(16-2)}{11} \geq R7 \geq 24$

$26.72 \geq R7 \geq 24$

Ⓑ B2 = $1/[(t_{cr})(R4+1) + (t_{sl})(R5)]$

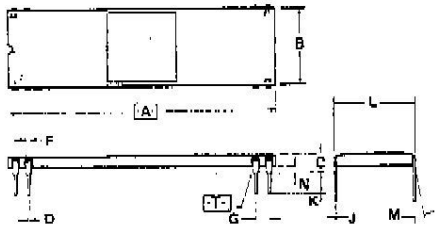
= $1/[(591.39 \times 10^{6})(28) + (53.76 \times 10^{-6})(2)]$

= $1/16.667 \times 10^{-3}$

= 60

PACKAGE DIMENSIONS

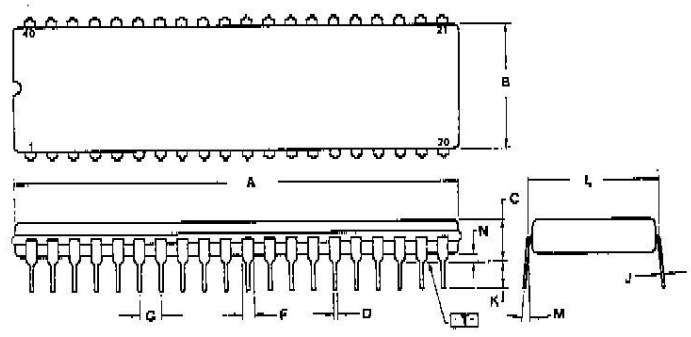
L SUFFIX
CERAMIC PACKAGE
CASE 715-05



NOTES:
1. DIMENSION A IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ 0.25 (0.010) M T A M
3. T IS SEATING PLANE.
4. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	50.29	51.31	1.980	2.020
B	14.83	15.49	0.576	0.610
C	2.79	4.32	0.110	0.170
D	0.38	0.53	0.015	0.021
F	0.76	1.62	0.030	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.33	0.008	0.013
K	2.54	4.57	0.100	0.180
L	14.99	15.65	0.590	0.616
M	–	10°	–	10°
N	1.02	1.52	0.040	0.060

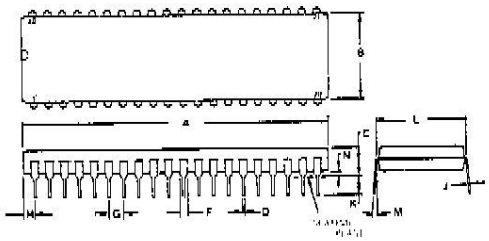
S SUFFIX
CERDIP PACKAGE
CASE 734-04



NOTES:
1. DIM A IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ Ø 0.25 (0.010) M T A M
3. T IS SEATING PLANE.
4. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONS A AND B INCLUDE MENISCUS.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51.31	53.24	2.020	2.096
B	12.70	15.49	0.500	0.610
C	4.06	5.84	0.160	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050

P SUFFIX
PLASTIC PACKAGE
CASE 711-03



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

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DS9826-R1

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MC6845 Addendum

ADDENDUM TO MC6845 CRT CONTROLLER (CRTC) Advance Information Data Sheet (DS-9838-R1)

Make the following changes to the MC6845 Data Sheet DS-9838-R1:

The clock frequency for "B" speed devices remains at 3.0 MHz. Standard and "A" speed devices now have a 2.5-MHz clock frequency. However, all devices having date codes between 8411 and 8428 were shipped with a 3-MHz character clock.

The CRTC TIMING CHARACTERISTICS table on page 5 should now read as follows:

CRTC TIMING CHARACTERISTICS (Reference Figures 4 and 5)

Characteristic	Symbol	MC6845 MC68A45 Min	MC6845 MC68A45 Max	MC68B45 Min	MC68B45 Max	Unit
Minimum Clock Pulse Width, Low	P_{WCL}	160	–	150	–	ns
Minimum Clock Pulse Width, High	P_{WCH}	200	–	150	–	ns
Clock Frequency	f_c	–	2.5	–	3.0	MHz
Rise and Fall Time for Clock Input	t_{cr}, t_{cf}	–	20	–	20	ns
Memory Address Delay Time	t_{MAD}	–	160	–	160	ns
Raster Address Delay Time	t_{RAD}	–	160	–	160	ns
Display Timing Delay Time	t_{DTD}	–	300	–	250	ns
Horizontal Sync Delay Time	t_{HSD}	–	300	–	250	ns
Vertical Sync Delay Time	t_{VSD}	–	300	–	250	ns
Cursor Display Timing Delay Time	t_{CDD}	–	300	–	250	ns
Light Pen Strobe Minimum Pulse Width	PW_{LPH}	100	–	80	–	ns
Light Pen Strobe Disable Time	t_{LPD1}	–	120	–	80	ns
	t_{LPD2}	–	0	–	10	ns

NOTE: The light pen strobe must fall to low level before VS pulse rises.

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