Ecolink Circuit Description

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1.0 Introduction

The following describes the operation of the Acorn Computer Ecolink Board. It will be necessary to refer to circuit diagram 0262,000/C, and the source listings for both of the PALs used on this board. Knowledge of the IBM PC's hardware is also a requirement.

The Ecolink board is a memory mapped peripheral for the IBM PC and compatibles it provides connection to the Acorn LAN Econet.

2.0 General Description

The Ecolink board contains the following functional blocks:

- PC Bus interface
- Dual-ported dynamic RAM DPRAM
- 65C12 microprocessor
- Non-volotile RAM (EEPROM)
- Econet interface
- There is also an optional EPROM which may be used to implement a discless workstation.

2.1 Block Description.

This section describes the various functional blocks and the ICs which make up those blocks.

2.1.1 PC Bus Interface.

IC's 26,27,28 and IC24d are Schmitt buffers, for address and control lines. Once buffered all PC address lines are refered to as 'Cnn' where nn is a number.

IC12 in association with IC22 (state machine PAL) provides Address decoding. IC22 ANDs the signal ADD with C19. for this board to be selected C19 must be high.

If the ROM option is used then the board uses 64K of PC address space. If not only 32K is used.

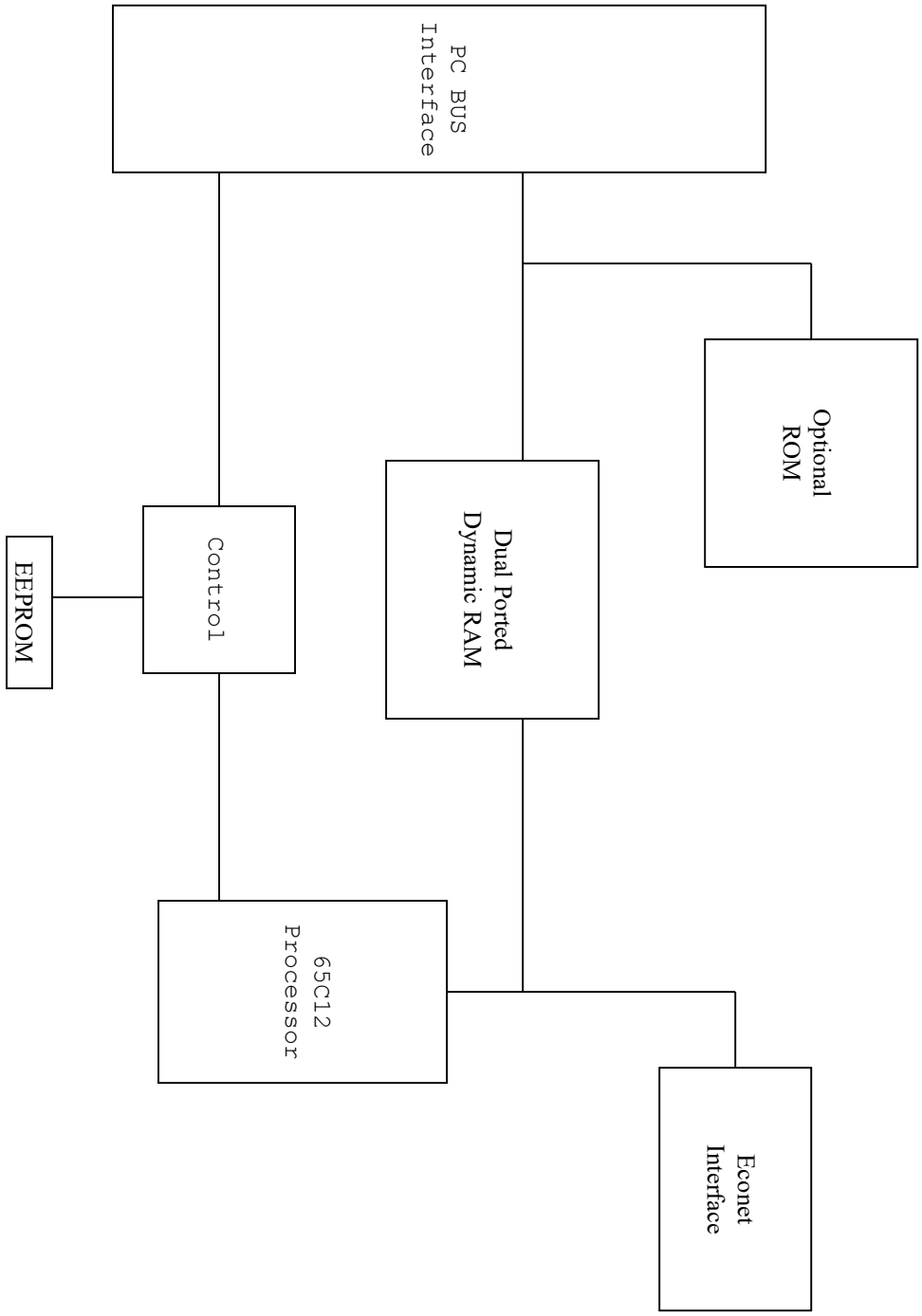
For operation without the ROM LINK 10 should be in the East position, connecting C15 to IC12. Thus C15 is used in address decoding. R9 ensures that the RAM input to IC22 remains high. This means that a /CAS strobe will always be issued during a PC cycle.
IC29 latches data from the DPRAM and holds it for the PC during a read cycle. IC 30 enables write data from the PC bus onto the internal data bus.

2.1.2 Control

This block consists of the two PALs some address decoding and the control latch. PAL IC22 (16R4) is programed as a state machine. Though the state variables RAS and TIM are provided externally by IC23. The third state variable is PHI2. State changes occur on the rising edge of OSC.

STATE	RAS	TIM	PHI2
A	0	0	1
B	1	0	0
C	1	1	0
D	0	1	0
E	0	0	1
F	1	0	1
G	1	1	1
H	0	1	1

State Table



MS DOS Econet Block Diagram
Rev. A
July 13, 1987

IC23 – has two functions:
1) synchronises the PC's memory read and write strobes, to the board's master clock (OSC), and
2) generates the signals RAS and TIM in quadrature phase. RAS leads TIM by 90DEG.

A request (REQ) is generated when the following equation is satisfied:

REQ = ADD*C19*WR + ADD*C19*RD

This means that the PC is making a read or write access to the Ecolink's memory area. The request is accepted for the next PHI2 low cycle.

Until the read or write request is satisfied the PC's bus cycle is extended using RDY.

The control area includes some address decoding used to detect accesses by either processor to the control latch. PAL IC21 controls the enables and strobes to generate the various types of bus cycle. See section 5.

2.2.3 DPRAM

The Dual Ported dynamic RAM is made up of two 64K by 4bit ICs, giving 64K bytes total. All nearly all 64K is available to the 6512 – some is lost to I/O. Only 32K of this RAM is available to PC this is to reduce Ecolink's occupation of PC address space. The RAM runs at twice the speed required by the 6512, this is so the PC may access the RAM without delaying the 6512.

2.2.4 EEPROM

A 128 bit EEPROM is included to provide storage for station number, file server number and printer server number. It is an IIC device, the read data from the EEPROM is only available to the 6512.

2.2.5 Econet Interface

An 6854 (ADLC) and line driver-receiver circuits provide connection to Econet. The Econet LAN runs a customised bit synchronous protocol. A bit clock is provided by the network.

2.3 Relative Speeds

The Ecolink board's master clock is 14.3181MHz taken from the "OSC" signal pin B30 on the PC edge connector. This saves an oscillator.

The 6512 runs at l.789MHz (14.3181MHz/8). The RAM runs at 3.579MHz [14.3181MHz/4]. This allows the use of 120nS RAS access DRAM. The 6512 uses every other RAM slot [cycle], This leaves half the slots available for use by the PC or to refresh the RAM.

2.2.1 RAM Refresh
Alternate RAM slots [cycles] are available for use by the PC. If a slot is not going to be used by the PC then it will be used to refresh the DRAM. There are two complete DRAM slots per cycle of PHI2.

As the PC's CPU loses its bus to its own DRAM refresh circuitry the Ecolink's DRAM is guaranteed sufficient refresh in the unused slots during

the PC's RAM refresh. The Ecolink board is not accessible to the PC's DMA unit. Note, one channel of a PC's DMA unit[s] is used to refresh its DRAM.

3.0 Address Mapping

The location and size of Ecolink within the PC s memory is dictated by the links LK1..4 and 10. See appendix A Link Settings.

3.1 ROM Operation.

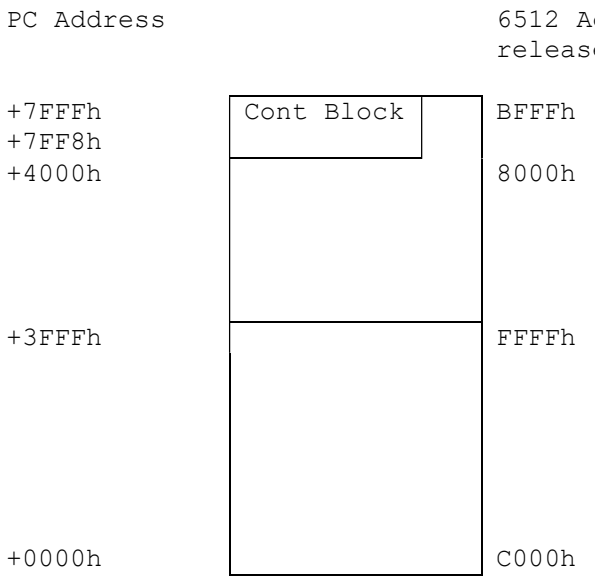
For ROM operation LK10 must connect C15 (buffered PC A15) to the signal RAM. In this mode Ecolink occupies 64K of PC address space. The lower 32K bytes are allocated to the optional ROM IC13, the upper 32K bytes are allocated to the Dual Ported RAM (DPRAM).
If ROM is not to be used then LK10 must must be made to connected to the address decoder IC12, RAM Will be pulled high. In this mode only 32K of PC address space is occupied.

3.2 DPRAM Paging

There are two possible DPRAM configurations available to the PC, selected by QO of IC19, Control latch offset 0 [see below). Using Q0 of the control latch different parts of the 6512's memory map are available to the PC through the 32Kbyte window:

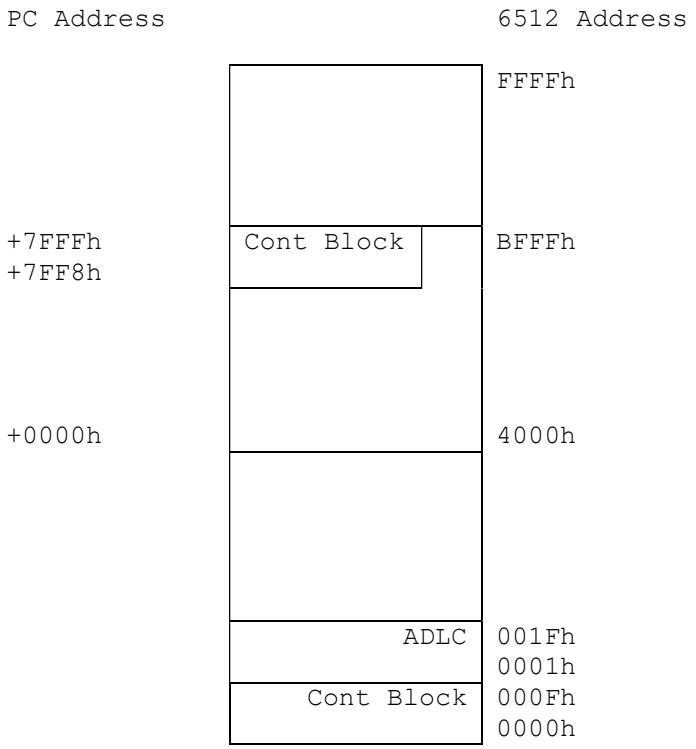
3.2.1 With 6512 Reset [IC19 Q0 = 0]

With Q0 = 0 -and hence the 6512 reset- the PC can access the top two quarters of the 6512's memory map. But in reverse order. At the bottom of the 32K window the memory that will become -when reset is released- the 6512's upper quarter [C000h to FFFFh] is accessible. This is so that the 6512's program can be loaded by the PC-.



With 6512 Reset

3.2.2 Without 6512 Reset [IC19 Q0 = 1]
Without the 6512 reset the PC can access the middle two quarters of the 6512's memory map. This is to facilitate data transfer between the two processors.



Without 6512 Reset

4.0 Control Block

Because of its lack of registers the 6512 requires an access sensitive control latch to dissable and re-enable NMI requests. To save components all the control registers operate in this way. Both processors require access to some of the bits in the latch. Thus it is dual ported, accessible from both the PC and the 6512.

4.1 Control Block Address Map

The Control Block is 8 bytes long but is double mapped in the 6512 memory map, and thus occupies 16 bytes of the 6512's zero page 0000h to 000Fh.

The Control Block occupies 8 bytes of the PC s memory map.

From PC BASE +	Operation			From 6512
	Read	Write	IC19	
	Latch ouput becomes 1	0		
7FF8h	6512 Reset off	on	QO	0000h
7FF9h	6512 IRQ off	on	Q1	0001h
7FFAh	PC INT on	off	Q2	0002h
7FFBh	------- Not used ---------		Q3	0003h
7FFCh	Serial Clock Raise	Lower	Q4	0004h
7FFDh	Serial Data Raise	Lower	Q5	0005h
7FFEh	6512 Cont Acc En Enable	Disable	Q6	0006h
7FFFh	NMI Enable Enable	Disable	Q7	0007h

The above table shows the location of registers within the control block and the effect of a read or write operation performed at a given location.
"Base +" Refers to the base address of the Ecolink Card.

Serial EEPROM data is recovered (6512 only) by reading location 0005h and examining data bit7. Ensure that Q5 has previously been set high, to allow the necessary set up time from "SDA" (see circuit) into the 6512.

5.0 Types of Bus Cycles

See Circuit Timing Diagram

5.1 Bus Cycles with PHI2 high

Durring PHI2 high the DPRAM and the internal data bus are at the disposal of the 6512. The 6512 uses this time to access the DPRAM, Control Block or the ADLC.

5.1.1 6512 DPRAM read

/RAS is active in states F and G. /CAS and /G are active in states G and H. /CAS may end (return high) at the end of state H, however if PC is not active it will remain low and perform a refresh cycle see 5.2.1 below.

5.1.2 6512 DPRAM write

As 6512 DPRAM read except that /W is asserted for the duration of PHI2 high, /W asserted disables /G.

5.1.3 6512 Control block read

The signals 65IO (high) and A4 (low) indicate to the peripheral PAL (IC21) that a control block access is required. The signal /W is taken as the data input to the addressable latch IC19.
During this cycle;

/G is not asserted.
The state of SDA is transfered to the data bus on D7, via the PAL.
/J259 is asserted during state G, this sets the Q output of IC19 addressed by N0..2.to a 1.

5.1.4 6512 Control block write

As 6512 Control block read except that PAL output D7 remains tristate and /W is low causing a 0 to appear at the addressed output of IC19. The contents of the data bus is written into DPRAM but at this address the DPRAM is write only!

5.1.5 6512 ADLC read

The signals 65IO (high) and A4 (high) indicate to the peripheral PAL (IC21) that an ADLC read is required. /ADLC is an asynchronous signal which is asserted when both 65IO and A4 are high. During this cycle /G is not asserted, the ADLC places the contents of the addressed register on the data bus.

5.1.6 6512 ADLC write

As 6512 ADLC read.

5.2 Bus Cycle with PHI2 low

PHI2 low bus cycles can be divided into two main types, refresh and those owned by the PC. The decision to allocate the next PHI2 low bus cycle, to the PC or refresh, is made at the end of the next to last state of PHI2 high, STATE G.

5.2.1 DPRAM Refresh

When in STATE H the signal PC is not asserted, a refresh will be performed in the next PHI2 low period. "Hidden refresh" mode is used, here /CAS remains low until after the next falling edge on /RAS. Both the /W /G signals will be inactive, and the data bus will be unused. The refresh address is provided by the RAM s internal counters.

5.2.2 PC DPRAM read
If a request (REQ) is outstanding at the end of STATE G then PC will be asserted in STATE H and will remain thus until the end Of STATE D. Asserting PC will switch the DPRAM address multiplexors over to the C (PC) address lines, and cause /CAS to return high at the end of STATE H. A normal DRAM read cycle will then ensue the resulting data will then be latched in to IC29, a transparent latch, when PC goes low. The signal /RBUF is active throughout the PC's read access. /G is active from STATE B to the end of STATE D, see ROM read.

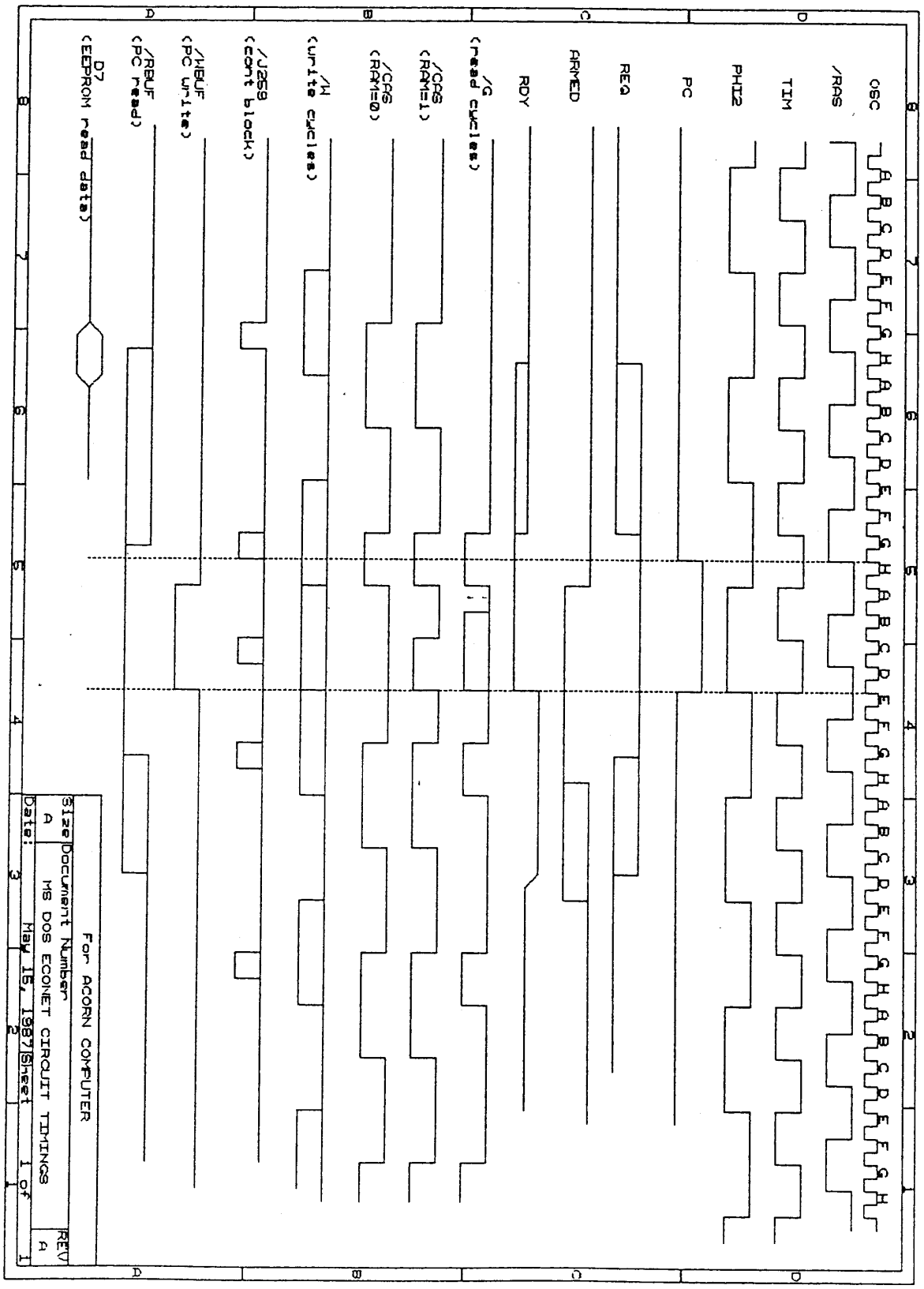
5.2.3 PC DPRAM write
This cycle is much the same as the PC DPRAM read except that /W and /WBUFF will be asserted for the duration of PHI2 low, /G will remain inactive. An "Early write" mode is used.

5.2.4 PC ROM read
Proceeds in much the same way as PC DPRAM read except that no /CAS signal is generated (this has the effect of turning off the RAM). The signal RAM will be low – indicating ROM. PC true and RAM false will enable the ROM's CE pin. The /G signal will be active from STATE B. This is one cycle earlier than it would be for a 6512 DPRAM read this allows the use of quite slow EPROMs.

5.2.5 PC ROM write
Not a very useful operation. No damage will result from this cycle as both ROM and DPRAM will be disabled. The PC's write data will be present on Ecolink s internal data bus.

5.2.6 PC Control block read
The signal /PCONT indicates to the peripheral PAL that a control block access is required. This cycle has the effect of setting the addressed control latch output high. It proceds in the same way as a PC RAM read except that /G is not asserted. The data bus contains no valid data.

5.2.7 PC Control block write
Has the effect setting the addressed control latch output low. It proceds in the same way as a PC RAM write. The data bus contains the PC's write data, which is written into the DPRAM. This data does not affect the output of control latch, and will only be readable from the 6512's side of the DPRAM.


OSC
/RAS
TIM
PHI2
PC
REQ
ARMED
RDY
/G (read cycles)
/CAS (RAM=1)
/CAS (RAM=0)
/W (write cycles)
/J2S9 (cont block)
/WBUF (PC write)
/RBUF (PC read)
D7 (EEPROM read data)
For ACORN COMPUTER
Size A
Document Number
REV A
MS DOS ECONET CIRCUIT TIMINGS
Date: May 15, 1987 Sheet 1 of 1

6.0 Optional ROM

IC position 13 is socketed to accept an optional 32K byte ROM. This ROM is only accessible from the PC.This ROM should conform to the definition for PC System-Accessible ROM Modules.

7.0 Econet Hardware

The circuitry used to provide connection Econet is an exact (including the layout) copy of the ECONET 2 MODULE, used in many Acorn products. A description of its operation is outside the scope of this document.

A Link Settings

FOR ISSUE B PCB

Links LK1 to LK4 control address:

X = Link IN . = Link OUT
E = East, SK1 9way cannon is at the east end of the board

No ROM operation.
- LK10 in normal position [connection nearest 9way Cannon made];
- 32k bytes of memory are consumed.

Address	LK4	LK3	LK2	LK1	LK10
F8000h- FFFFFh	.	.	.	.	E
F0000h- F7FFFh	.	.	.	X	E
E8000h- EFFFFh	.	.	X	.	E
E0000h- E7FFFh	.	.	X	X	E
D8000h- DFFFFh	.	X	.	.	E
D0000h- D7FFFh	.	X	.	X	E
C8000h- CFFFFh	.	X	X	.	E
C0000h- C7FFFh	.	X	X	X	E
B8000h- BFFFFh	X	.	.	.	E
B0000h- B7FFFh	X	.	.	X	E
A8000h- AFFFFh	X	.	X	.	E
A0000h- A7FFFh	X	.	X	X	E
98000h- 9FFFFh	X	X	.	.	E
90000h- 97FFFh	X	X	.	X	E
88000h- 8FFFFh	X	X	X	.	E
80000h- 87FFFh	X	X	X	X	E

ROM Operation
- LK10 in the other position [connection away from 9way Cannon made] NB the ROM will be mapped in, and 64K bytes of memory will be consumed 32K for ROM and 32K RAM.

For this type of operation LK1 MUST be out.

Address	LK4	LK3	LK2	LK1	LK10
F0000h- FFFFFh	.	.	.	.	W
E0000h- EFFFFh	.	.	X	.	W
D0000h- DFFFFh	.	X	.	.	W
C0000h- CFFFFh	.	X	X	.	W
B0000h- BFFFFh	X	.	.	.	W
A0000h- AFFFFh	X	.	X	.	W
90000h- 9FFFFh	X	X	.	.	W
80000h- 8FFFFh	X	X	X	.	W

Note the board is designed to support a 32K byte ROM. If certain 16K byte

EPROMs are installed, they may not appear in the memory in the lower 16K address space, they will appear from: Base address + 4000h.

Links LK5-8,11,12 select [PC's] Interrupt channels.
Note only ONE of these links should be installed.

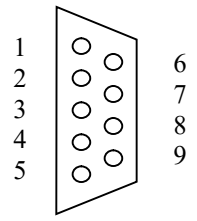
LK12 selects IRQ7
LK11 selects IRQ6
LK5 selects IRQ5
LK6 selects IRQ4
LK7 selects IRQ3
LK8 selects IRQ2

Signal Connector

Econet connector, mounted at the rear of the board,

9 WAY D-type Cannon Socket:

Pin	Signal
1	+data
2	-data
3	Gnd
4	+clk
5	-clk
6	Gnd
7	Gnd
8	Gnd
9	Is Special*



View from rear of Ecolink

Pin 9: Normally 0V, LK9 will allow +5V to be brought out on this pin. LK9 is not fitted and requires its normal connection to be cut if the +5V option is to be used.

Instructions for Modification to Ecolink (AEH30)

The following modification is to be used on all Ecolink Cards supplied prior to the 10th November 1987 to rectify a configuration problem, all units supplied after this date will NOT require this modification.

Modify Issue 1 Boards as per attached sketch, this involves 1 cut and 2 links. Replace C7 47pF with 82pF. Cut solderside adjacent R12 between two "via" holes. Link "via" hole linking IC16 pin 1, with IC15 pin 12,13. Link IC5 pin 2 to IC15 pin 11. Please remember to complete a service report and submit it to the Warranty Control Group as normal.