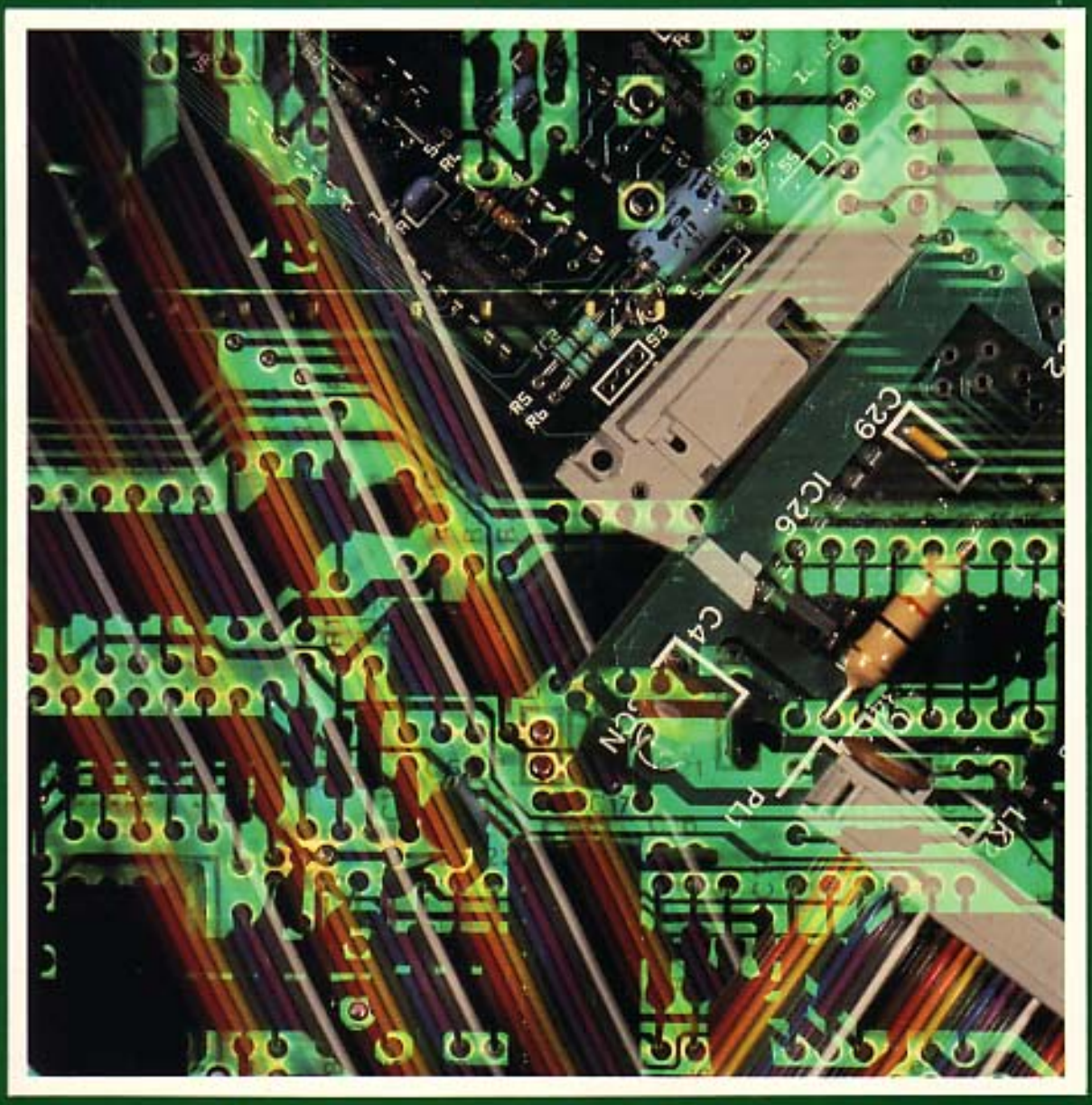
ACORN COMPUTER

Z80 second processor

Service Manual



Z80 SECOND PROCESSSOR SERVICE MANUAL

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is detected. IC26 and IC27 provide a clock signal, $\overline{\text{NMISERV}}$ during such a cycle, which presets the ROM latch IC15A, latching the ROM in until an instruction-fetch from high RAM. In the ROM, 66H contains a jump to the destination expected by standard CPM.

5.4 Wait-states

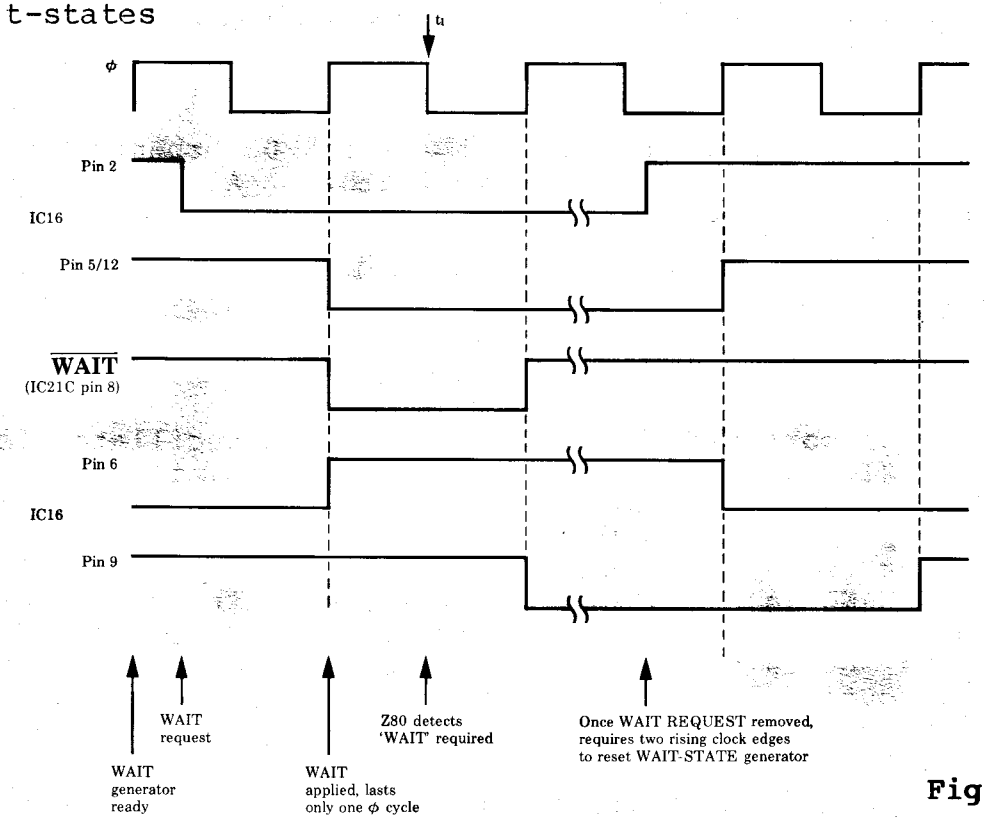


Fig. 1

Because of the slow access time of the "boot" ROM, all memory cycles to the ROM must be lengthened by the insertion of a "Wait-State" of one clock cycle. When the ROM is selected, the OR gate IC22C provides the $\overline{\text{OE}}$ signal to the ROM and this is used to enable the Wait-State generator IC16A&B. Via the NAND gate IC21C, a low-going pulse of 1 clock cycle is fed to the $\overline{\text{WAIT}}$ input of the Z80 (see timing diagram above). The Wait generator requires a further two clock cycles after the end of the lengthened memory cycle to clear itself. The Z80 samples the $\overline{\text{WAIT}}$ input on the falling edge of ϕ (t_1). TP7 allows observation of the $\overline{\text{WAIT}}$ signal.

5.5. Reset

The Z80 second processor may be reset at any time, by the host processor via the Tube.

The Z80 requires that a reset signal should not occur immediately after an instruction fetch cycle, otherwise corruption of DRAM data might result. To avoid this, the "D" latch IC15B synchronises the reset signal from the Tube to the beginning of an instruction-fetch cycle ($\overline{\text{M1}}$). A monostable IC14 ensures the reset

signal to the CPU is a pulse of approx. 4µs duration, sufficient to produce a reset without delaying the refresh to the DRAMS and so losing data. The reset to the CPU also clears the ROM latch IC15A, bringing the shadow ROM into the memory-map.

The Schmitt NAND gate IC19C provides a Power-Up reset to the Z80 from the delay network R1, C2 (time-constant 100ms). Diode D1 ensures that the capacitor does not apply a reverse voltage to the NAND gate input on Power-Down.

5.6 Interrupt Handling

The host processor can interrupt the Z80 with a maskable interrupt via the Tube. The interrupt output from the Tube is taken directly to the INT input of the Z80. After detection of an interrupt, the CPU $\overline{M1}$ and $\overline{IORQ}$ outputs go low to indicate a vector for the interrupt is expected on the data bus D0 to D7. The buffer IC28 is enabled by $\overline{M1}$ and $\overline{IORQ}$ and its inputs are permanently tied to logic 0 or 1 to give a vector address of 0FEH. The Z80 'Boot' ROM places the Z80 internal interrupt system into Mode 2, with a High-Byte address of 0FFH, giving an address for the interrupt vector of 0FFFEH.

5.7 DRAM Control

5.7.1 Read/Write Cycles

a. $\overline{RAS}$

Whenever a memory cycle occurs, the preset signal on the "D" latch IC17B is removed by the $\overline{MREQ}$ signal from the Z80. On the next rising edge of the system clock, the "D" latch output goes low, giving the "CHOP" signal. During memory read or write cycles, the falling edge of CHOP produces the row-address ($\overline{RAS}$) signal (TP8), via IC20A, to the DRAMS, causing the row address information to be latched by the RAMS. Prior to the $\overline{RAS}$ signal, the row-address buffer IC5 was enabled by the high level on $\overline{RAS}$ and consequently the low level on the inverted $\overline{RAS}$ signal from IC21A, thus allowing the low order address lines A0 to A7 to be passed to the DRAMS. Once $\overline{RAS}$ goes low, IC5 is disabled and IC4 enabled, to allow the column address through to the DRAMS. The inverter IC25E ensures a slight delay in the enabling of the Column buffer, to avoid data conflict with the Row buffer.

b. $\overline{CAS}$

The column-address signal to the DRAMS is generated from the $\overline{RAS}$ signal by the OR gates IC23C&D. If the shadow ROM output-enable signal is active, then the $\overline{CAS}$ signal will not be generated (logic 1 on pin 12 - IC23D). The AND gate IC20C enables or disables the $\overline{CAS}$ signal under certain other conditions.

$\overline{CAS}$ is enabled if:

i. the memory cycle is a write cycle ($\overline{WR}$ low, to IC20C pin 11).

or ii. the memory cycle is a read cycle and not an instruction-fetch cycle (IC18B not preset by $\overline{M1}$, RED signal to IC20 pin 9).

or iii. the cycle is an instruction-fetch this signal being synchronised to the CHOP signal by OR gate IC23B (to IC20 pin 10)

Note: In this case, the $\overline{CAS}$ signal will not be generated if the ROM is selected.

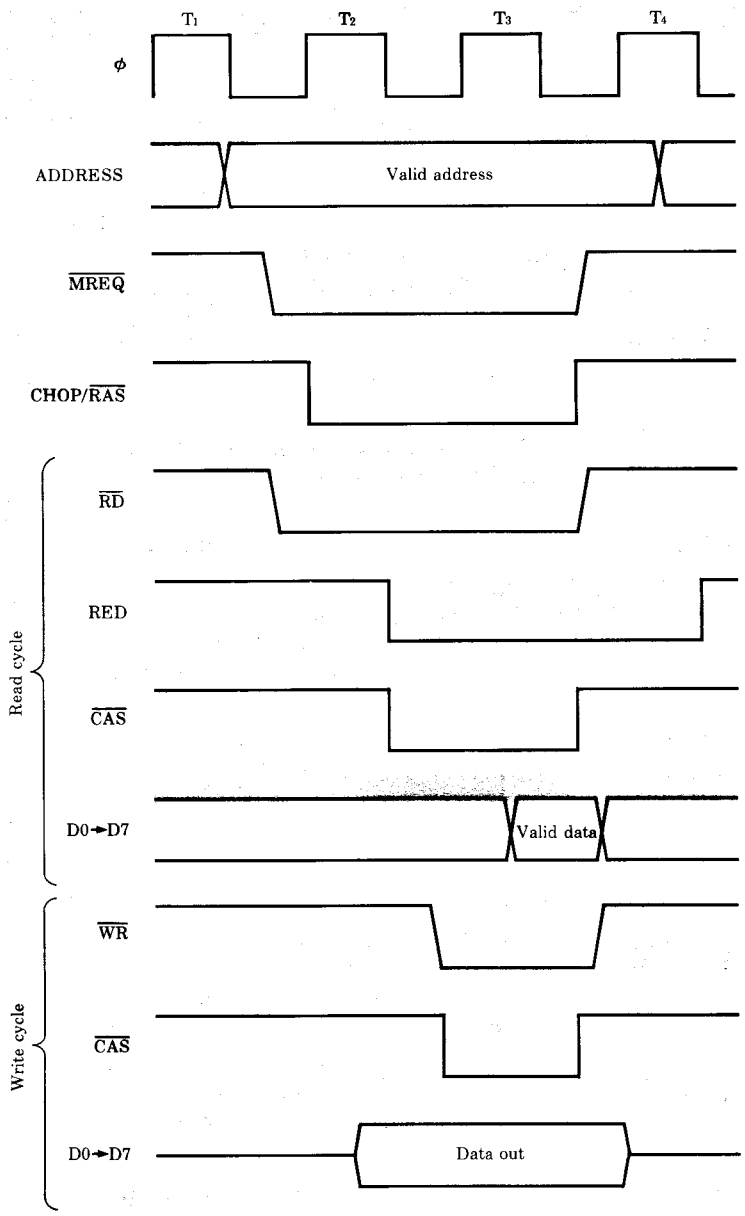


Fig. 2 RAM read or write cycles

5.7.2 Instruction-Fetch Cycles

The Z80 CPU handles an Instruction Fetch differently to other memory read cycles, in that the $\overline{MREQ}$ signal is active for only 1.5 clock cycles instead of 2. In order to allow sufficient access time for the DRAMS in this abbreviated cycle, the Instruction-Fetch signal, $\overline{M1}$, is used to generate the $\overline{RAS}$ and $\overline{CAS}$ signals a half-cycle earlier. The OR gate IC23A allows the clock signal through to the "D" latch IC18A, only when $\overline{M1}$ is active. The output of the "D" latch, SUE is clocked low, and generates the row-address latch signal $\overline{RAS}$, a half clock cycle before the CHOP signal would have done. When the CHOP signal arrives after being generated by the $\overline{MREQ}$ (see section 5.7.1a), it clears the SUE latch and holds $\overline{RAS}$ low itself until $\overline{MREQ}$ becomes inactive.

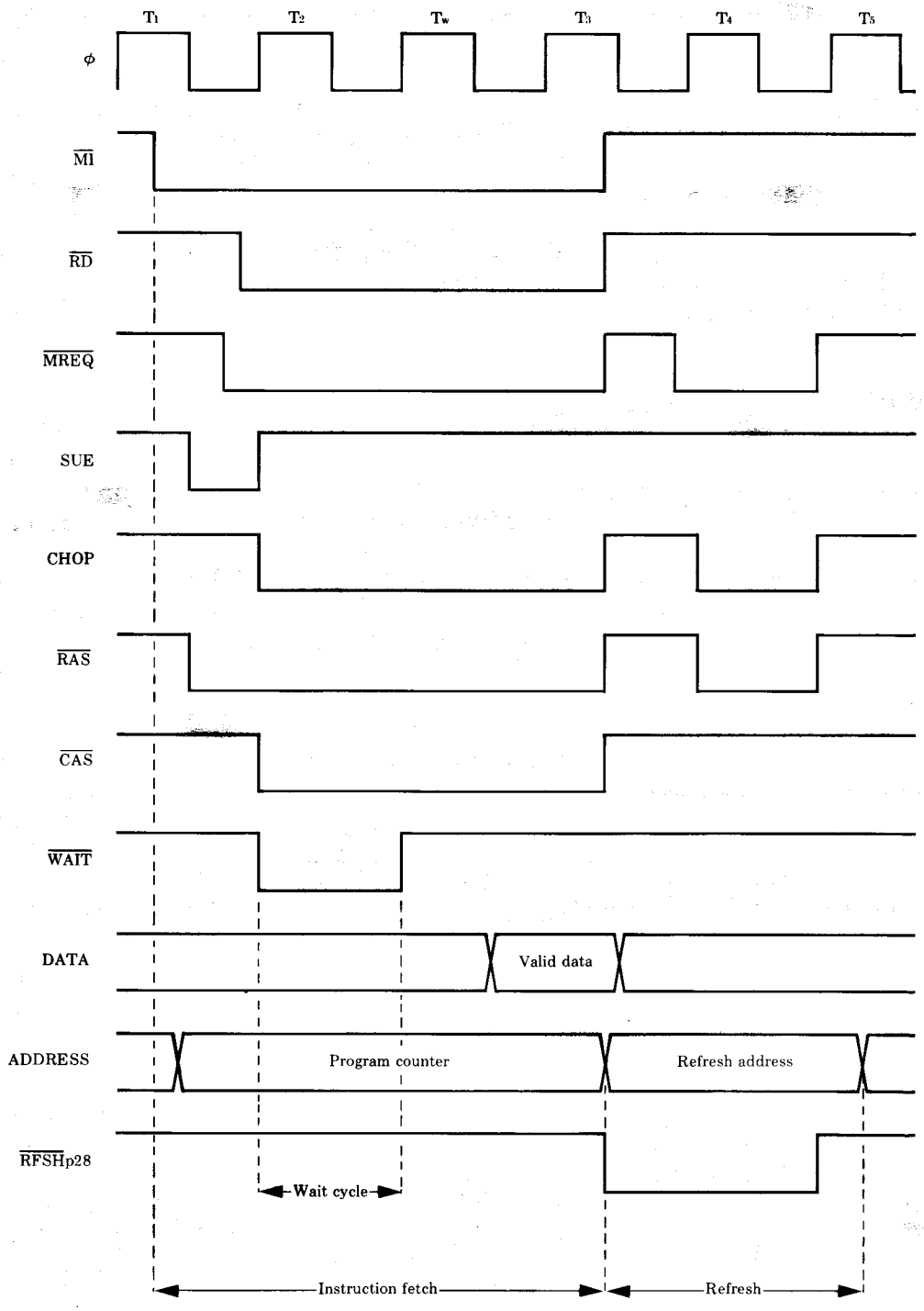


Fig. 3 Instruction-Fetch cycles

5.8 DRAM Refresh

After each instruction-fetch, the Z80 CPU performs a Refresh cycle for the DRAMS in the period while the instruction is being decoded. A seven-bit refresh address is output onto the address-bus (A0 to A6, A7 =0) for approx. 2 clock cycles, and the MREQ signal goes low. The "RFSH" signal from the Z80 is not used, and no other

memory control signals go active. The Refresh address is incremented by the CPU after each time.

Once the $\overline{MREQ}$ signal goes active, the "D" latch IC18B produces CHOP and hence $\overline{RAS}$ as normal. The $\overline{CAS}$ is not required for a Refresh cycle, and is not enabled since none of the conditions listed in section 5.7.1b are true (AND gate IC20C).

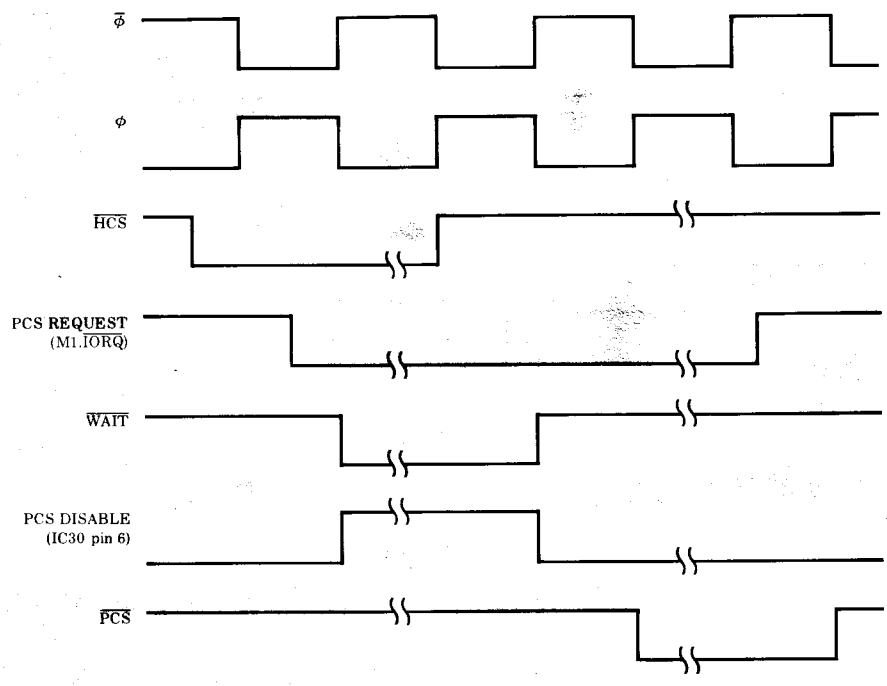
When the shadow ROM is being read, the $\overline{CAS}$ signal to the DRAMS is disabled, but the row-address latch signal, $\overline{RAS}$, still occurs. This has the effect of a refresh cycle to the DRAMS.

5.9 Desynchronising Logic

To prevent ambiguous events, i.e. a register status change during a status read, this circuit produces a "WAIT" signal to the Z80 processor when the $\overline{PCS}$ and $\overline{HCS}$ signals occur simultaneously.

When this happens, a low signal from IC29B pin 6 appears at IC30A pin 2. Q on IC30A goes high and, via IC29A, maintains a logic 1 signal upon pin 12 of IC30B, thus, by the end of one clock cycle a high is sent from pin 9 of IC30B to disable $\overline{PCS}$. Simultaneously, a $\overline{WAIT}$ signal is generated for the second processor via IC19A&B.

As soon as $\overline{HCS}$ (TP6) is removed, the next rising clock edge removes the $\overline{WAIT}$ signal from the Z80 and, as $\overline{PCS}$ is still low, a low signal is sent through IC30B to the Tube. This is then maintained by the low signal upon pin 4 of IC30A until the $\overline{PCS}$ is complete.



HCS disables PCS until HCS completed

Thus, if $\overline{PCS}$ (TP5) is already running, it will continue despite an $\overline{HCS}$, but if $\overline{HCS}$ began first then $\overline{PCS}$ is prevented from acting.

*At no time is $\overline{HCS}$ affected, as it would not be possible to 'stop' the BBC processor.

Fig. 4 Timing Diagram - $\overline{HCS}/\overline{PCS}$

5.10 The Tube

The Tube (IC1) is an Acorn custom IC which provides parallel asynchronous communication between two processor systems, the BBC Microcomputer (Host) and the Z80 second processor (Parasite). To each processor system, it resembles a conventional peripheral device comprising 4 read-only and 4 write-only, 8-bit registers. The Z80 accesses these registers via its I/O structure.

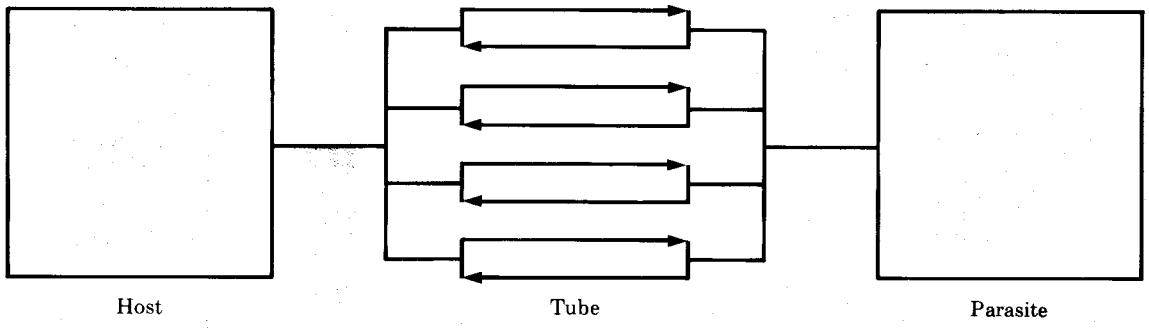


Fig. 5 Tube concept

5.10.1 Tube Registers

Each register has its own status byte, with a separate I/O address, containing Register-Full and Data-Available flags. The status byte for Register 1 contains additional control bits that may be set by the Host computer to enable interrupts or to reset the Z80. These control bits may be read, but not set, by the second processor.

Fig. 6 shows the Tube registers in more detail

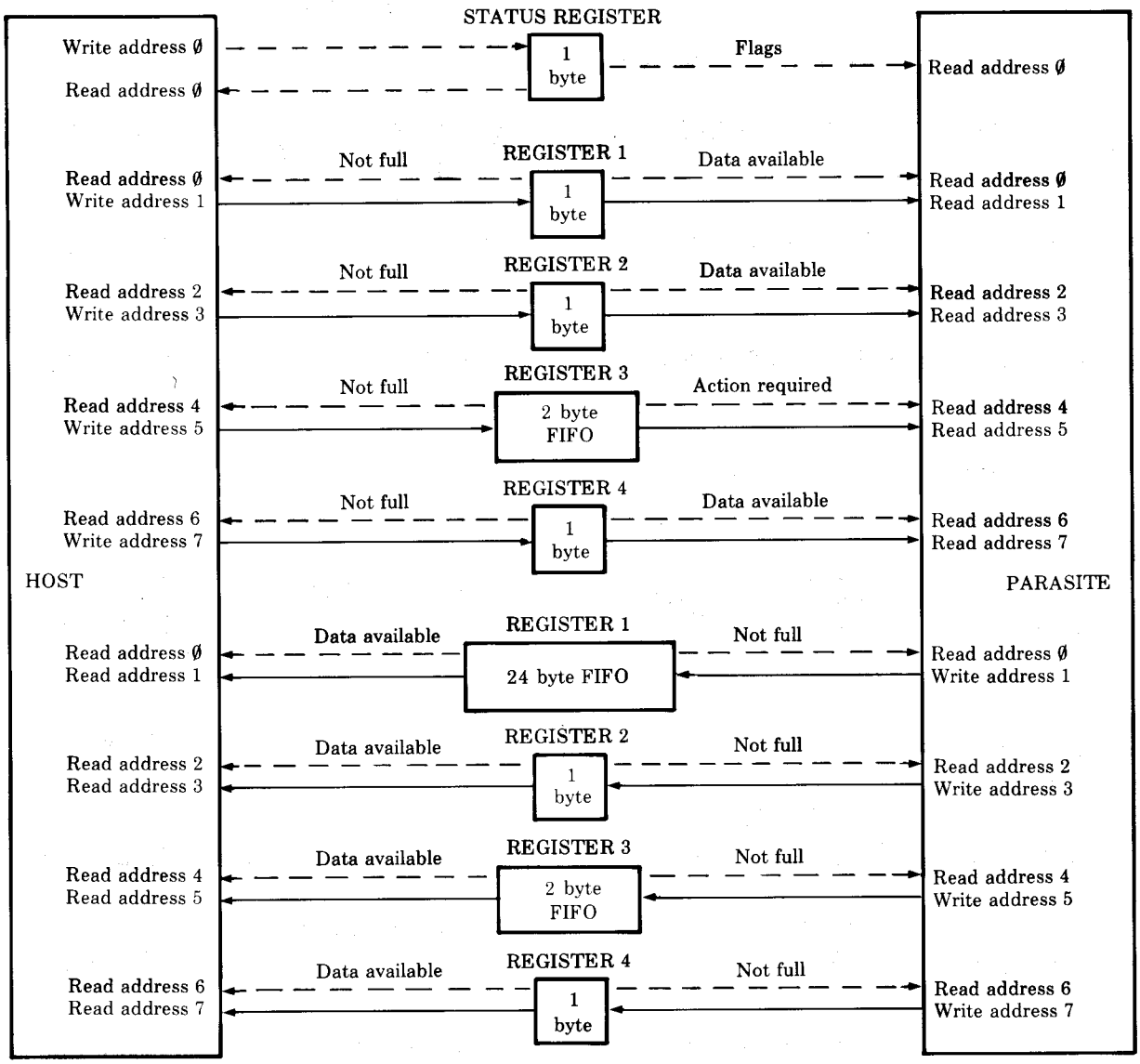


Fig. 6 Schematic diagram of Tube registers

The following tables show the relative address and type of each register in the Tube, firstly for the Host system, and secondly for the parasite system (second processor).

Table 1 Host system registers

Address	Read
000	Status flags and Register 1 flags
001	Register 1 (24 byte FIFO read only)
010	Register 2 flags
011	Register 2 (1 byte read only)
100	Register 3 flags
101	Register 3 (2 byte FIFO read only)
110	Register 4 flags
111	Register 4 (1 byte read only)

Address	Write
000	Status Flags
001	Register 1 (1 byte write only)
010	------
011	Register 2 (1 byte write only)
100	------
101	Register 3 (2 byte FIFO write only)
110	------
111	Register 4 (1 byte write only)

Table 2 Parasite system registers

Address	Read
000	Status flags and Register 1 flags A1 F1 P V M J I Q
001	Register 1 (1 byte read only)
010	Register 2 flags
011	Register 2 (1 byte read only)
100	Register 3 flags
101	Register 3 (2 byte FIFO read only)
110	Register 4 flags
111	Register 4 (1 byte read only)

Address	Write
000	------
001	Register 1 (24 byte FIFO write only)
010	------
011	Register 2 (1 byte write only)
100	------
101	Register 3 (2 byte FIFO write only)
110	------
111	Register 4 (1 byte write only)

As can be seen from Fig. 6 and Tables 1 and 2, each numbered register (e.g. register 1) is actually two registers, one for reading and one for writing. The register selected is determined by R/W on the Host system and by NRDS/NWDS on the Parasite system (see Tube Pinout Diagram).

Only registers 2 and 4 are simple latches; register 3 is a 2-byte FIFO in each direction and register 1 is a 24-byte FIFO from the Parasite (Z80) to the Host, but a simple latch from Host to the Parasite. The Tube produces maskable and non-maskable interrupts to the Parasite (see sections 5.6 and 5.3) and a reset signal (section 5.5).

The Z80 $\overline{\text{IORQ}}$ and $\overline{\text{M1}}$ signals are decoded to detect an I/O cycle by the OR gate IC22A, which provides the signal which, via the De-sync circuit, initiates the chip-select, $\overline{\text{PCS}}$, to the Tube. The Tube thus occupies all of the Z80 I/O map, the four data registers and four associated status registers reflecting throughout the possible 256 addresses.

5.10.2 Tube Pinout

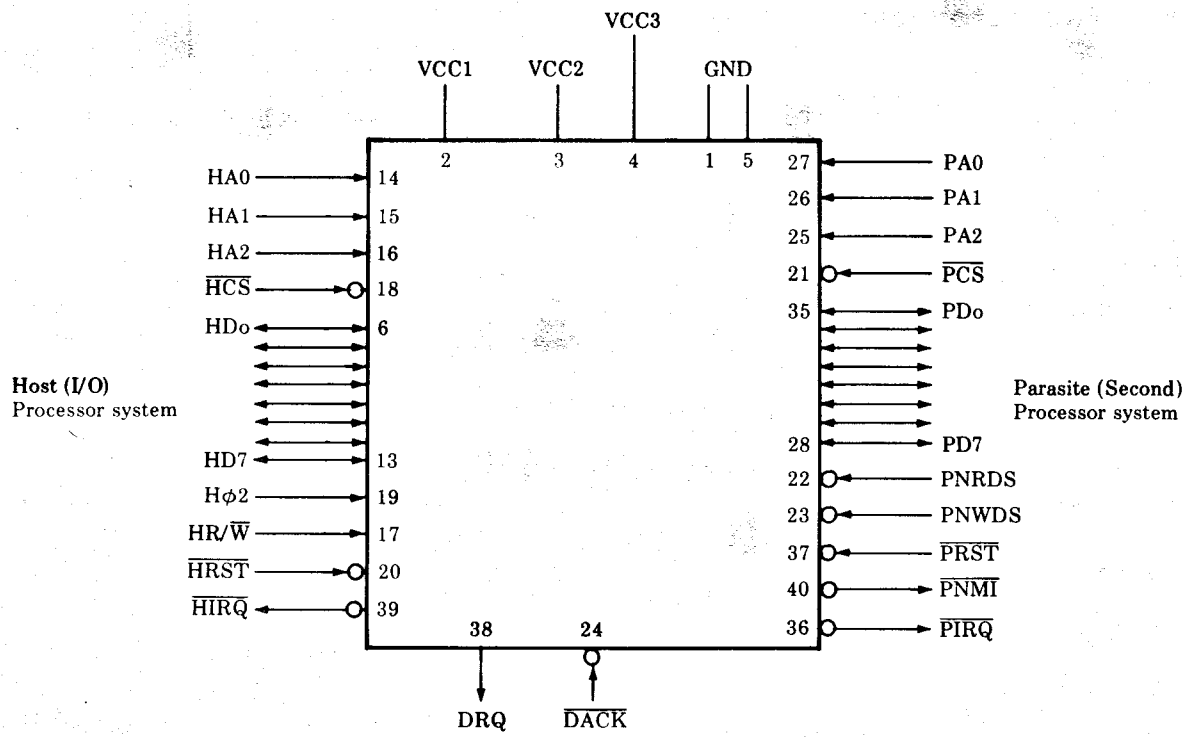


Fig. 7 Pinout diagram for Tube IC

DESCRIPTION OF PINS (ref. Fig.7):

Power Supply	GND	0V supply rail
	VCC1	Parasite main +5V supply
	VCC2	Parasite secondary supply (+2-3v)
	VCC3	Host +5V supply
Data buses	HD0-7	8-bit data bus to Host processor
	PD0-7	8-bit data bus to Parasite processor
Address signals	HA0-2	3 register select lines from Host
	PA0-2	3 register select lines from Parasite
	$\overline{HCS}$	Host chip select
	$\overline{PCS}$	Parasite chip select
Timing signals	Hϕ2	Host ϕ2 - high level signifies valid address bus
	HR/$\overline{W}$	Host read/write line - determines whether read or write register is selected on address specified by HA0-2, and direction of data flow on HD0-7
	PNRDS	Parasite read strobe (active-low)
	PNWDS	Parasite write strobe (active-low)
Interrupt lines	$\overline{HRST}$	Host reset (RST) -initialises Tube to known state and generates $\overline{PRST}$
	$\overline{PRST}$	Reset (RST) line to parasite processor
	$\overline{PNMI}$	Non-maskable interrupt to parasite
	$\overline{HIRQ}$	Interrupt to Host (not used by Z80 second processor)
DMA lines	$\overline{DRQ}$	Request for DMA transfer
	$\overline{DACK}$	DMA acknowledge from DMA controller

DMA facility is not used by the Z80 second processor

Within this publication the term 'BBC' is used as an abbreviation for 'British Broadcasting Corporation'.

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5.10.3 Tube Timing Diagram

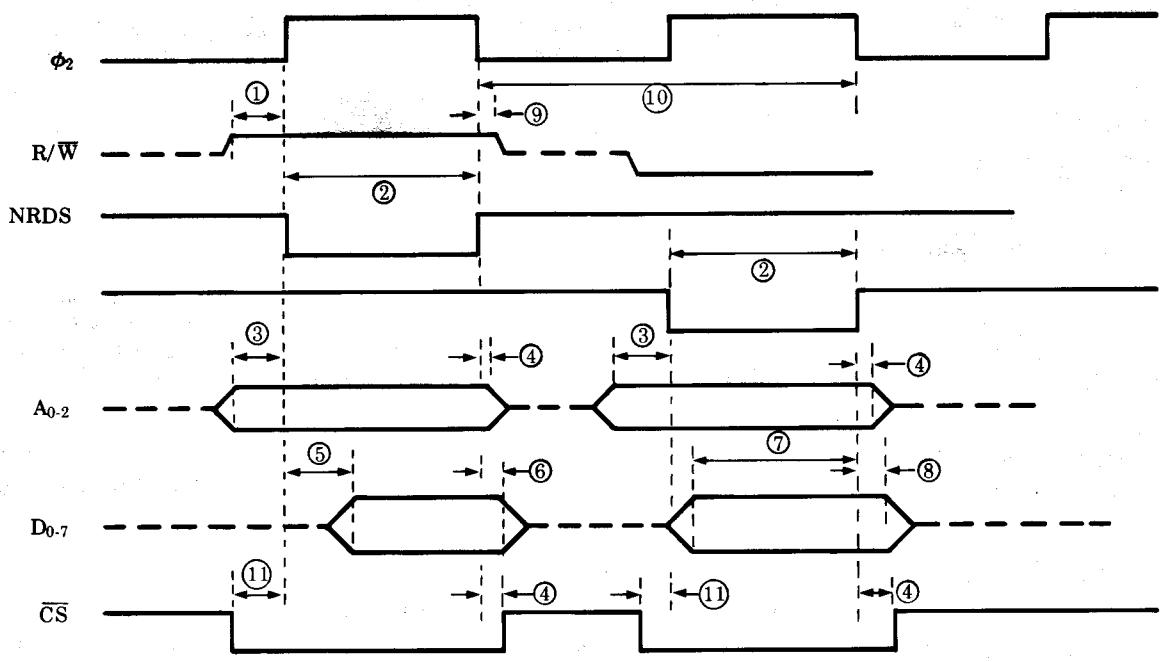


Fig. 8 Tube Timing Diagram

N.B. The timing reference for the Host is ϕ2 and R/$\overline{W}$ gives the direction of transfer.
For the parasite, the PCS direction is given by PNRDS or PNWDS, and timing by PCS.

		MIN	MAX
1	R/$\overline{W}$ SET UP TO ϕ2	35ns	
2	TIMING STROBE PULSE WIDTH	110ns	
3	ADDRESS SET UP TIME	35ns	
4	ADDRESS & CHIP SELECT HOLD TIMES	10ns	
5	DATA OUT DELAY TIME		70ns
6	DATA OUT HOLD TIME	10ns	
7	DATA IN SET UP TIME	50ns	
8	DATA IN HOLD TIME	20ns	
9	R/W HOLD TIME	10ns	
10	CYCLE TIME	250ns	
11	CS SET UP TIME	20ns	

6. Fault Finding on the Z80 Second Processor

6.1 General

a) The Z80 second processor has three socketed IC's (IC 1 - 3) - these may easily be replaced if necessary.

b) Test points are provided on the Z80 PCB, as follows:

TP1	CLOCK	6MHz clock signal ϕ to pin 6 of Z80 processor
TP2	ROM	disable/activate signal to ROM, pins 18 & 20
TP3	$\overline{M1}$	Z80 generated clock signal indicating an instruction-fetch cycle. Also used in interrupt handling.
TP4	$\overline{MREQ}$	goes low to indicate memory addressing
TP5	$\overline{PCS}$	indicates successful parasite chip select to Tube, via de-sync logic circuit
TP6	$\overline{HCS}$	indicates Host chip select to tube
TP7	$\overline{WAIT}$	Occurs during reads from the ROM and as result of simultaneous HCS/PCS event. Enables refresh cycles
TP8	$\overline{RAS}$	Row Address Signal, used in ALL memory addressing, both for accessing and refreshing
TP9	$\overline{CAS}$	Column Address Signal, used only for memory accessing, disabled during refresh

6.2 Fault Conditions

A Z80 Second Processor failure can usually be related to one of five fault conditions:

"BBC Microcomputer 32k..." message displayed.

Predominantly caused by either power failure, misconnected or damaged plugs and/or interconnecting cable.

"Acorn TUBE Z80 64k ..." message displayed; no response to Keyboard.

If this message is displayed, the ROM has been copied completely to RAM , the ROM disabled and the Boot procedure begun. Failure to respond to the keyboard means that the system has crashed due to either hardware or software failure. Possible causes may be:

Software	**Hardware**
Incompatible or failed	Tube register fault
DNFS or Boot ROM	Z80 fault
	DRAM error

A further consideration is that a component or components may have become temperature sensitive and are failing intermittently. Check by first replacing IC1, IC2 and IC3 in turn, then check operation once warm; use a freezer spray to locate temperature-sensitive components.

Flashing Cursor in the top left corner of an otherwise blank screen (Total Failure)

This is the most usual result of plugging in a broken Z80 second processor as the majority of faults manifest themselves in this way.

Normal Operation until BREAK reset attempted; system fails.

Most probably caused by failure of reset circuit (IC15b, IC14 and associated components).

BBC Microcomputer fails when Z80 Second Processor connected to Tube socket

Probable causes are misconnected or damaged plugs/sockets and/or damaged ribbon cable; Tube IC failure or IC29 failed on Z80 PCB.

Diagnostic Flowcharts for the above conditions are given in the Appendix. These should be read in conjunction with the following Circuit Checks:

6.3 Circuit Checks

6.3.1 Clock

Using an oscilloscope, check that a 12MHz signal is being generated at pin 13 of IC22D. If not, check the crystal X1, resistor values and operation of inverters IC24D/E. Trace the signal to pin 9 of IC17A where it should appear as a clearly defined 6MHz square wave ($\overline{\phi}$). ϕ should appear from the driver Q1 to supply IC2 pin 6. Check that the clock signals, ϕ and $\overline{\phi}$ appear at all the expected points shown on the circuit diagram. If not, check for loading caused by failed IC's and track short- circuits. Pin 11 of IC19D should also be generating a delayed clock required for the $\overline{\text{NMISERV}}$ circuit. If no delayed clock is found, check the values of C9 and R9.

6.3.2 RAS/CAS Generator Circuits

Both of these are best traced back from the RAM. $\overline{\text{RAS}}$ is always present and should be seen at TP8 and also inverted at pin 3 of IC21A. If only one appears, then check for loading, either on the address buffers or on the DRAMS.

$\overline{\text{RAS}}$ is generated by both IC18A and IC17B (SUE and CHOP signals respectively), independently of each other, but both are required to be operating for full $\overline{\text{RAS}}$ ability. $\overline{\text{RAS}}$ may therefore be appearing due to only one of the two Dtypes working, so check that pins 1 and 2 of both IC20A and IC21A are operating. If not, check the operation of the Dtypes according to inputs; $\overline{\text{RAS}}$ will fail if the CPU is not operating as it requires $\overline{\text{M1}}$, and $\overline{\text{MREQ}}$, as well as the clock signal.

The operation of $\overline{\text{CAS}}$ is dependant upon the functioning of $\overline{\text{RAS}}$ and also the correct decoding of a memory access. Check that memory $\overline{\text{RD}}$, $\overline{\text{W}}$ or Instruction Fetch ($\overline{\text{M1}}$) signals appear then check that this is properly decoded from IC23B to IC23C via IC20C, and not disabled by an incorrect signal from IC23D.

6.3.3 Wait State Generator

IC2 pin 24 should predominantly be high; WAIT should only be active under two conditions:

i) During ROM read, TP2 goes low for approximately 0.25sec. This is visible as a low on a logic probe applied to IC16A pin 2 after the BREAK key has been pressed.

ii) When HCS and PCS occur simultaneously; this WAIT pulse is generated frequently during data transfer via the Tube. Note that, in this second case, the $\overline{\text{WAIT}}$ signal is produced by the desync. logic.

If $\overline{WAIT}$ is permanently low, or high, check TP7 after pressing BREAK; the $\overline{WAIT}$ signal should go low and then high. If not, check that ϕ is clocking IC16A and B and IC30A and B (for $\overline{HCS}/\overline{PCS}$ $\overline{WAIT}$) and that the desync. circuits are producing the correct $\overline{WAIT}$ outputs. See section 5.9.

6.3.4 ROM Signal/Break

On power-up, the RC network R1, C2, D1 provides a low to high transition of approximately 0.1 second duration to pin 9 of IC19C. If power-up reset fails and the low to high transition time is found to be incorrect, check these component values and replace as necessary.

After power-up, pressing and releasing the BREAK key on the host keyboard causes $\overline{PRST}$ to appear on pin 37 of Tube IC1. This is clocked through IC15B by $\overline{M1}$. Thus, if the CPU is halted for any reason, $\overline{M1}$ will not be present and a BREAK reset will not be possible, i.e. a successful power-up reset is necessary to allow any further resets to work.

The low signal should clock to monostable IC14 which should produce a signal of approximately 10µs duration. If not, check the values of RC network R7/C8 and replace if necessary.

The output of IC14 appears at pin 10 of IC19C; from here on the reset function is common to both power-up and BREAK, as follows:

The reset signal from IC19C is inverted by IC24F and appears at pin 26 of IC2 (CPU reset) and also at pin 3 of IC 15A (ROM latch) so that, if IC15A is functioning correctly, a reset should cause a low-going pulse to appear at IC2 pin 26 (reset active low), followed by a low on TP2 ($\overline{ROM}$). This signal must appear at pin 18 of IC3 and requires both $\overline{MREQ}$ and $\overline{RD}$ to be both active low to pass IC22C and output enable IC3 on pin 20 (and disable $\overline{CAS}$ at IC21D, pin 13).

The active-low $\overline{ROM}$ signal at IC22C also appears at pin 2 of IC16A which enables $\overline{WAIT}$ states at pin 24 of IC2 (see Wait State Generator, above). Using an oscilloscope, check that all these events occur, replacing any failed components.

After $\overline{ROM}$ on TP2 has remained low for approximately 0.25s, the CPU executes an instruction fetch from high memory, $\overline{M1}$ and $\overline{MREQ}$ both go to active low and their inverted signals appear at pins 3 and 5 respectively of IC20B. This, combined with A15 high should produce a low at pin 6 which, via IC24C will clear IC15A at pin 1 and remove the $\overline{ROM}$ signal. Again, check all conditions with an oscilloscope and correct any failed logic.

6.3.5 Desynchronising Logic and PCS Disable

$\overline{HCS}$

After power-up, check that $\overline{HCS}$ is active at pin 18 of IC1. If not, then either the Tube IC1 or IC29 has failed on the second processor side, there is a ribbon cable/connector fault, or the Host is faulty.

$\overline{PCS}$

After pressing BREAK, check that a low signal appears simultaneously at pins 1 and 2 of IC22A and that this appears at pin 3. Check that a low then appears at pin 21 of IC1; if not, the Desync. logic circuit is faulty. Check the clock signal at pin 11 of IC30 and the inverted clock signal at pin 3. Whilst referring to the Circuit Description, check that all signals are operating correctly in the Desync. logic circuit.

With $\overline{HCS}$ checked to be functioning correctly, $\overline{PCS\ REQ}$, via IC29A, should always reach Pin 12 of IC30B when HCS is high. If not, check operation of IC30A and that pin 5 of IC30A only produces a low signal when $\overline{HCS}$ is active.

6.3.6 $\overline{NMISERV}$

When an active signal appears at pin 17 of IC2 ($\overline{NMI}$), the address lines should be seen to address 066H (instruction fetch). This should decode through IC26/27 to give the $\overline{NMISERV}$ signal. Failure of this circuit will prevent disk access. If this occurs, check ϕD clock circuit, that $\overline{NMI}$ from IC2 pin 17 appears at pin 5 of IC21B and that $\overline{NMISERV}$ from pin 9 of IC27 appears at pin 4 of IC15A and IC21D pin 12. Check for broken tracks and replace IC's 26 and 27 if necessary.

6.3.7 Interrupt 0FEH

When operating the Boot ROM, the interrupt vector 0FEH from IC28 will be read. Check the operation of IC28, that $\overline{M1}$ and $\overline{IORQ}$ are appearing, that the buffer inputs are correctly tied (high or low) and that the buffer output of "FE" is appearing upon request; if not, check tracks and power rails. Replace IC28 if necessary.

6.3.8 DRAMS (Dynamic RAM IC's)

The following should be performed for each DRAM in turn (IC's 6 - 13):
Check the power supply pins, +5v to pin 8 and 0v to pin 16. Check that $\overline{RAS}$, $\overline{CAS}$, and $\overline{W}$ are all appearing, then make sure that address buffers become enabled (active low) at pins 1 and 19 of IC's 4 and 5,and providing active address lines to the DRAMS. Check that no

address lines are shorted together and that all data lines are operating and not tied together.

6.3.9 Power Supply

Check the 250 mA. type T mains fuse, accessible at the rear of the unit (see section 2).

Check for any loose, disconnected or broken leads.

After making sure that the second processor is disconnected from the mains supply, check the mains switch at the rear of the unit.

Overload protection of the second processor is provided on the second processor Z80 board itself. Fuse FS1 protects against overcurrent and thyristor TH1 protects against overvoltage by blowing the fuse.

The overvoltage protection circuit functions as follows:

D3 is a 5.1V Zener diode; rail voltages greater than 5.1V appear across resistor R11 whilst spikes are absorbed by capacitor C11. If the rail voltage across R11 exceeds approximately 1V, thyristor TH1, which is capable of drawing 8 amps., conducts and blows the 1 amp. fast-blow fuse FS1. Supply rail cut-off is therefore achieved if the voltage reaches approximately 6.1V.

If fuse FS1 is blown, it could be due to either overvoltage or overcurrent and there is likely to be either a short circuit somewhere or the power supply board is faulty (it is supplying too high a voltage).

Disconnect the two power supply leads, brown and black, from the second processor PCB and connect a 10 ohm 2.5W resistor between them. Measure the voltage across the brown lead (+5V) and the black lead (ground) which should be in the range 4.95 to 5.25V with a maximum of 50mV noise (peak-to-peak, 0-50MHz bandwidth). If the voltage is out of spec. then set it to 5V exactly using the trimmer which is accessible through a hole in the power supply board. See Fig. 9.

If 5v cannot be obtained and/or the noise level is out of spec., replace the power supply unit.

Now remove the resistor connected across the power supply leads and reconnect them to the second processor PCB, ensuring correct polarity. Test the current drawn by the second processor PCB from the +5V supply. The board should draw 600 - 800mA from the power supply.

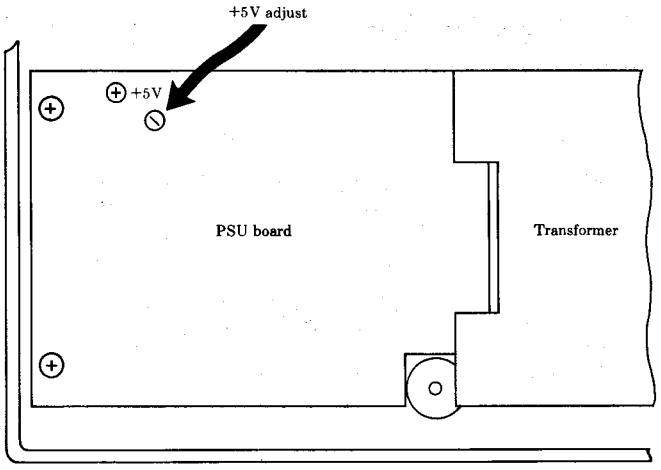


Fig. 9 Position of +5V Trimmer on Power Supply PCB.

If the current is zero, the second processor PCB has gone open circuit. Check fuse FS1 and connectors and tracks.

If the fuse is blown, the fault is a short circuit on the PCB.

If the current is higher than it should be, measure the voltage. If the voltage is greater than 5.25V, adjust it to 5V using the trimmer- see fig. 9. If the voltage is in spec., then one or more of the components on the second processor PCB is faulty. Switch off the power supply and feel which of the components is hot.

WARNING TAKE CARE WHEN CHECKING FOR 'HOT' COMPONENTS - THEY MAY BE HOT ENOUGH TO CAUSE INJURY.

6.3.10 Checking the Tube power supplies

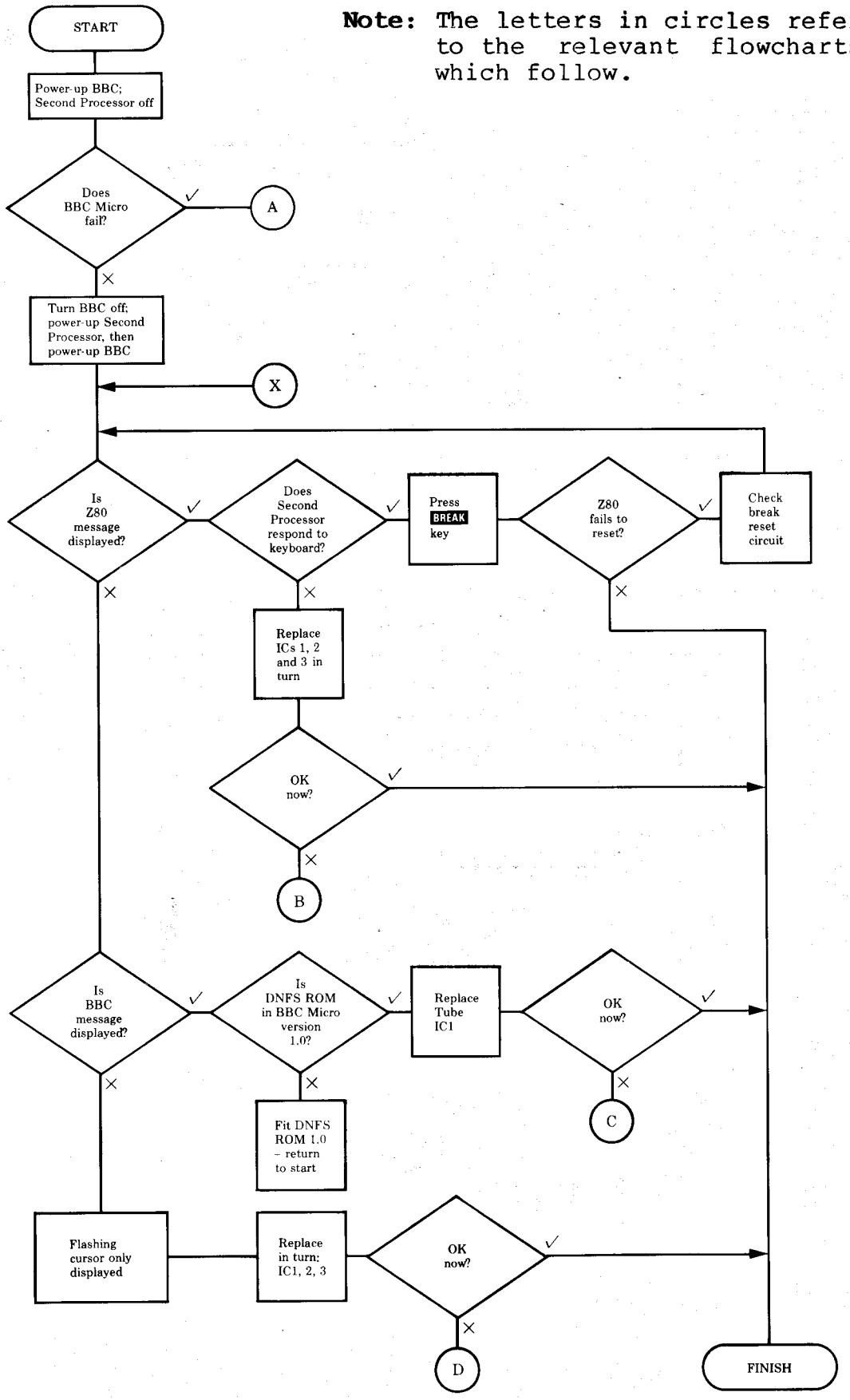
The Tube (IC1) is powered both from the BBC Microcomputer and from the second processor. If either of these supplies fails then the second processor will not work.

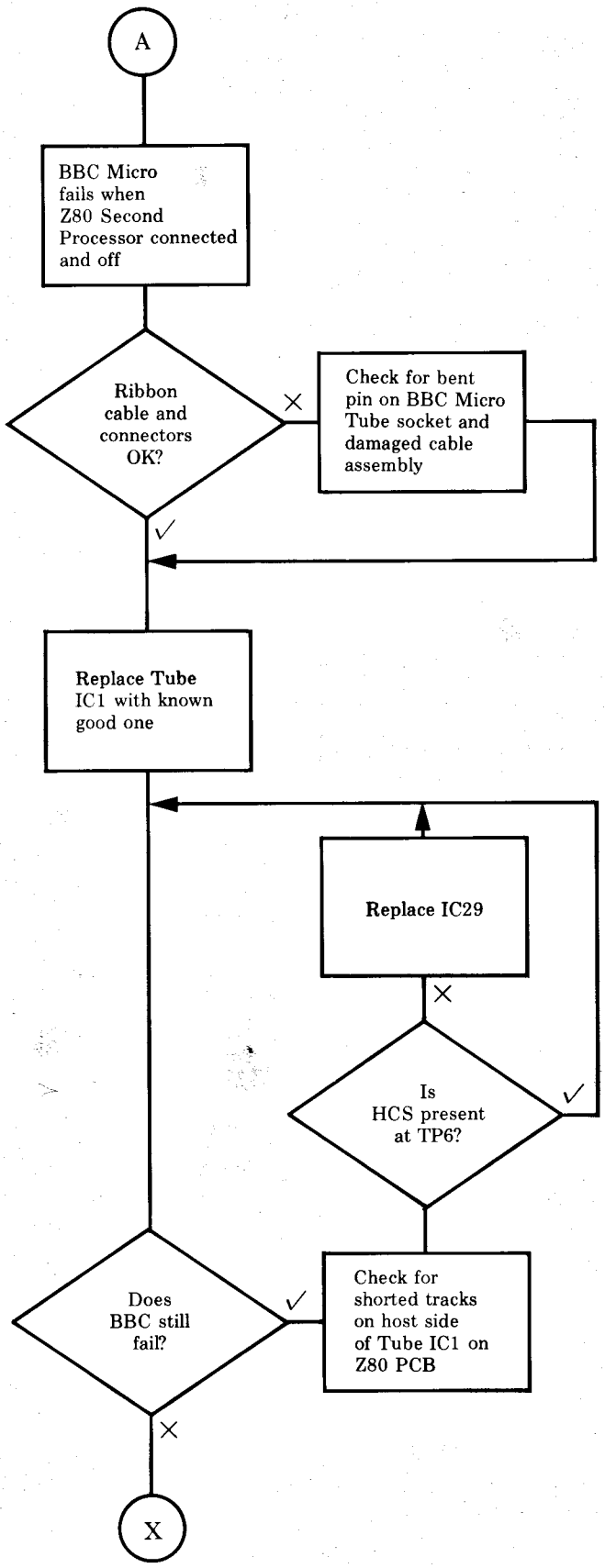
With the second processor switched off (ON/OFF switch down), switch on the BBC Microcomputer (ON/OFF switch up). Check that there is a potential of approx. 5V between pin 4 (+ve) and pins 1 and 5 (ground) of IC1. If not, check the ribbon cable and connectors.

Now switch off the BBC Microcomputer (ON/OFF switch down), and switch on the second processor (ON/OFF switch up). Check that there is a potential of 5V between pin 2 (+ve) and pins 1 and 5 (ground) of IC1. Also, check that there is a potential of between +2v and +3v between pin 3 and both pins 1 and 5. If not, investigate components R2 and L1, replacing if necessary.

Diagnostic Flowcharts

Note: The letters in circles refer to the relevant flowcharts which follow.




A
BBC Micro fails when Z80 Second Processor connected and off
Ribbon cable and connectors OK?
Check for bent pin on BBC Micro Tube socket and damaged cable assembly
Replace Tube IC1 with known good one
Replace IC29
Is HCS present at TP6?
Check for shorted tracks on host side of Tube IC1 on Z80 PCB
Does BBC still fail?
X

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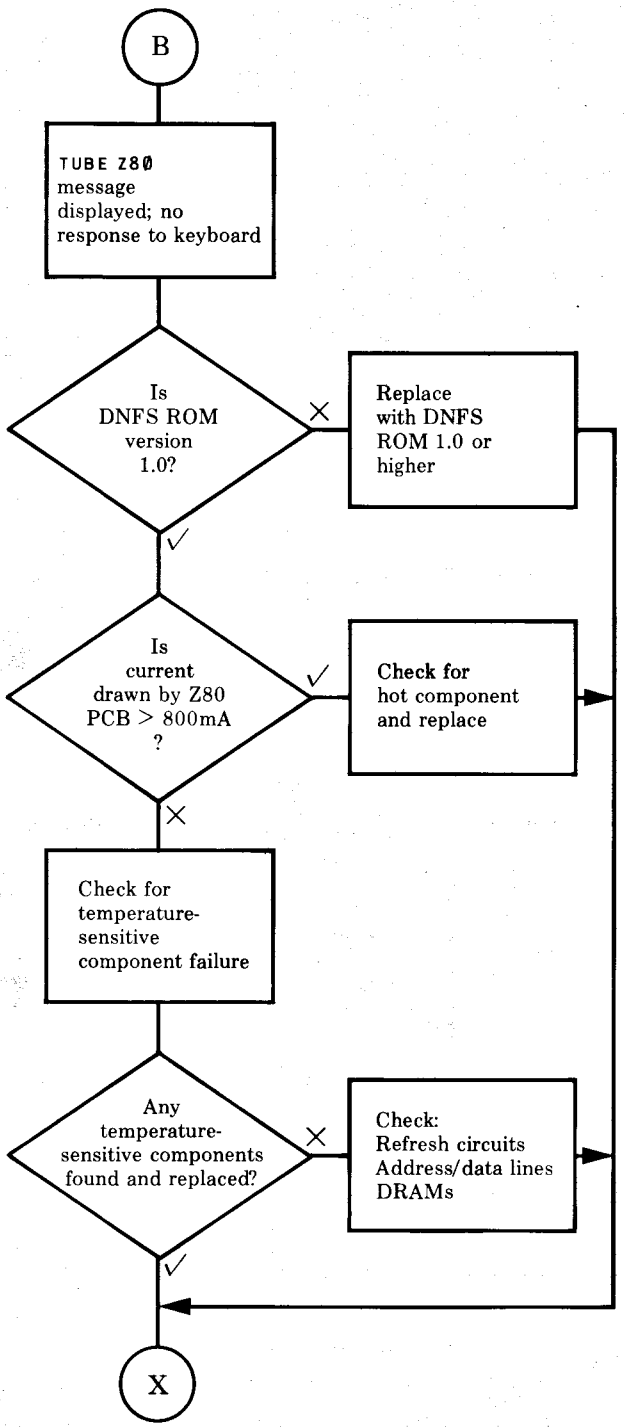
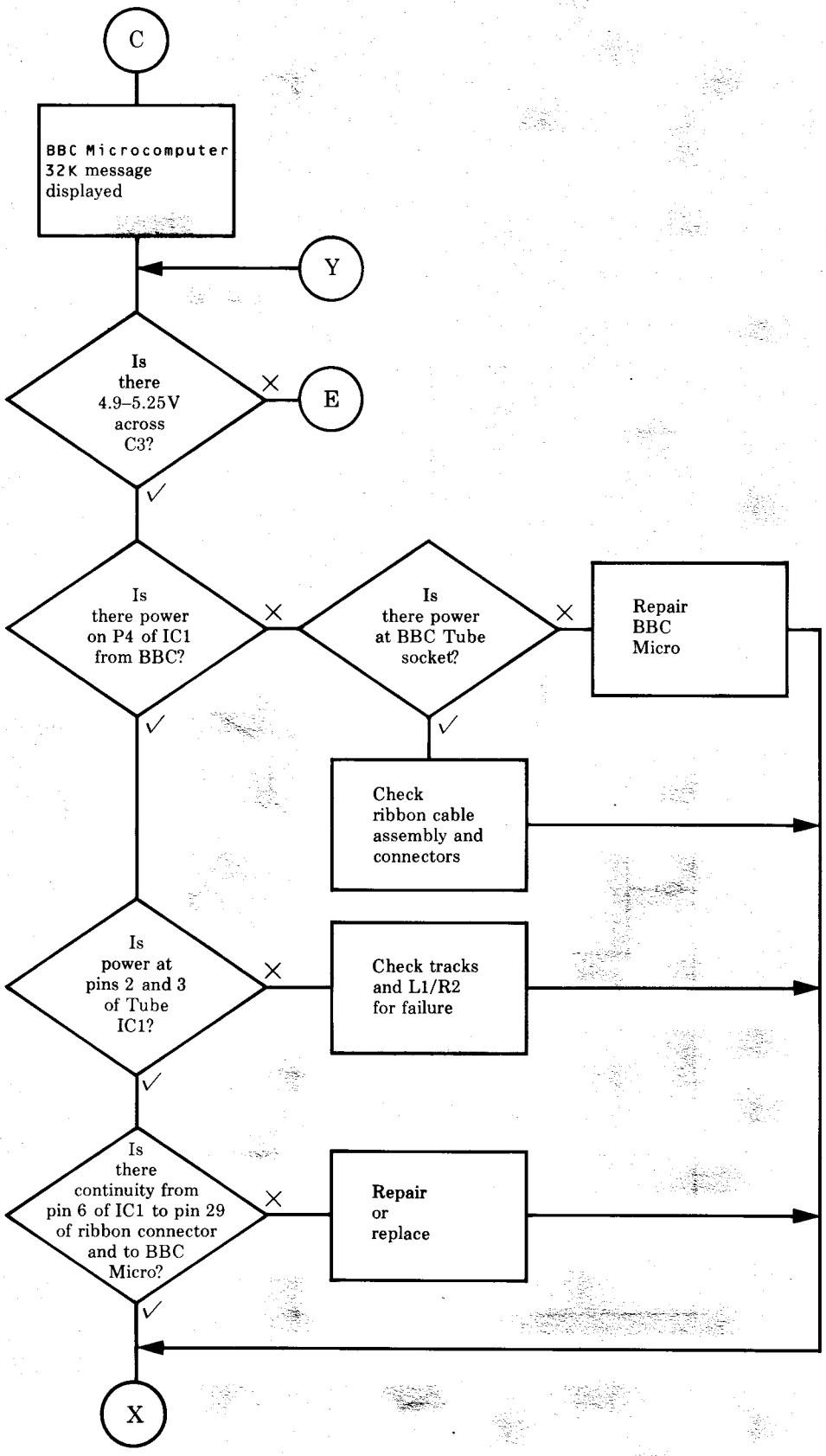
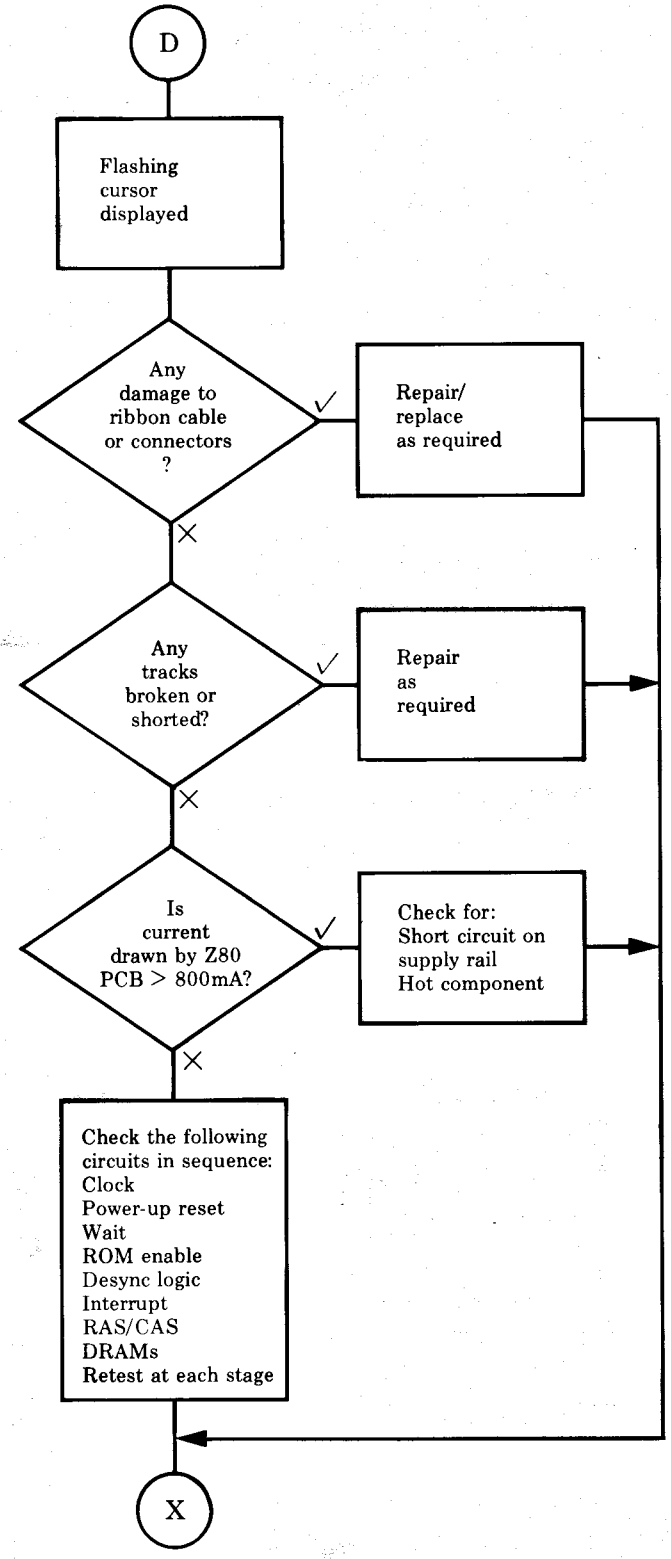
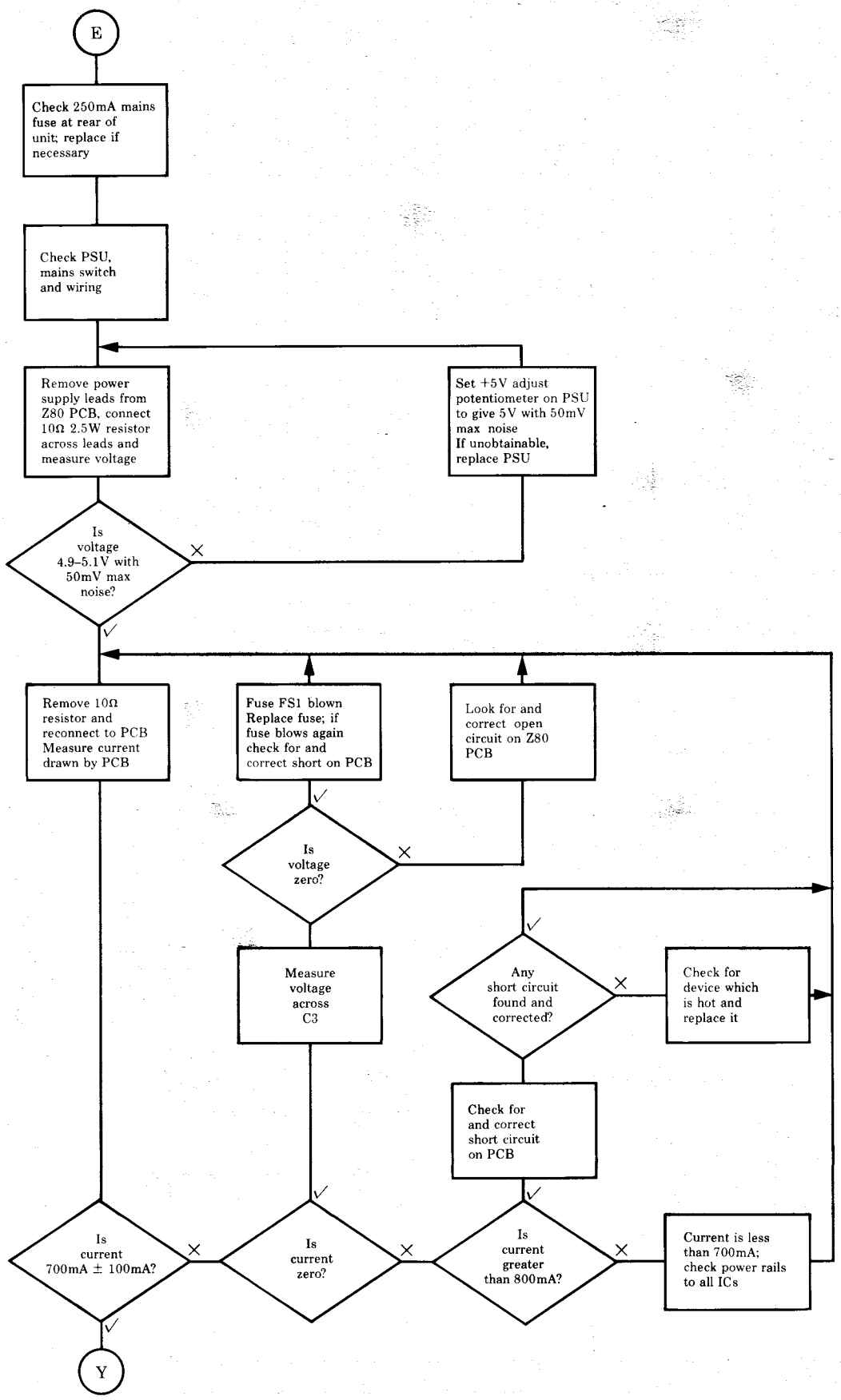
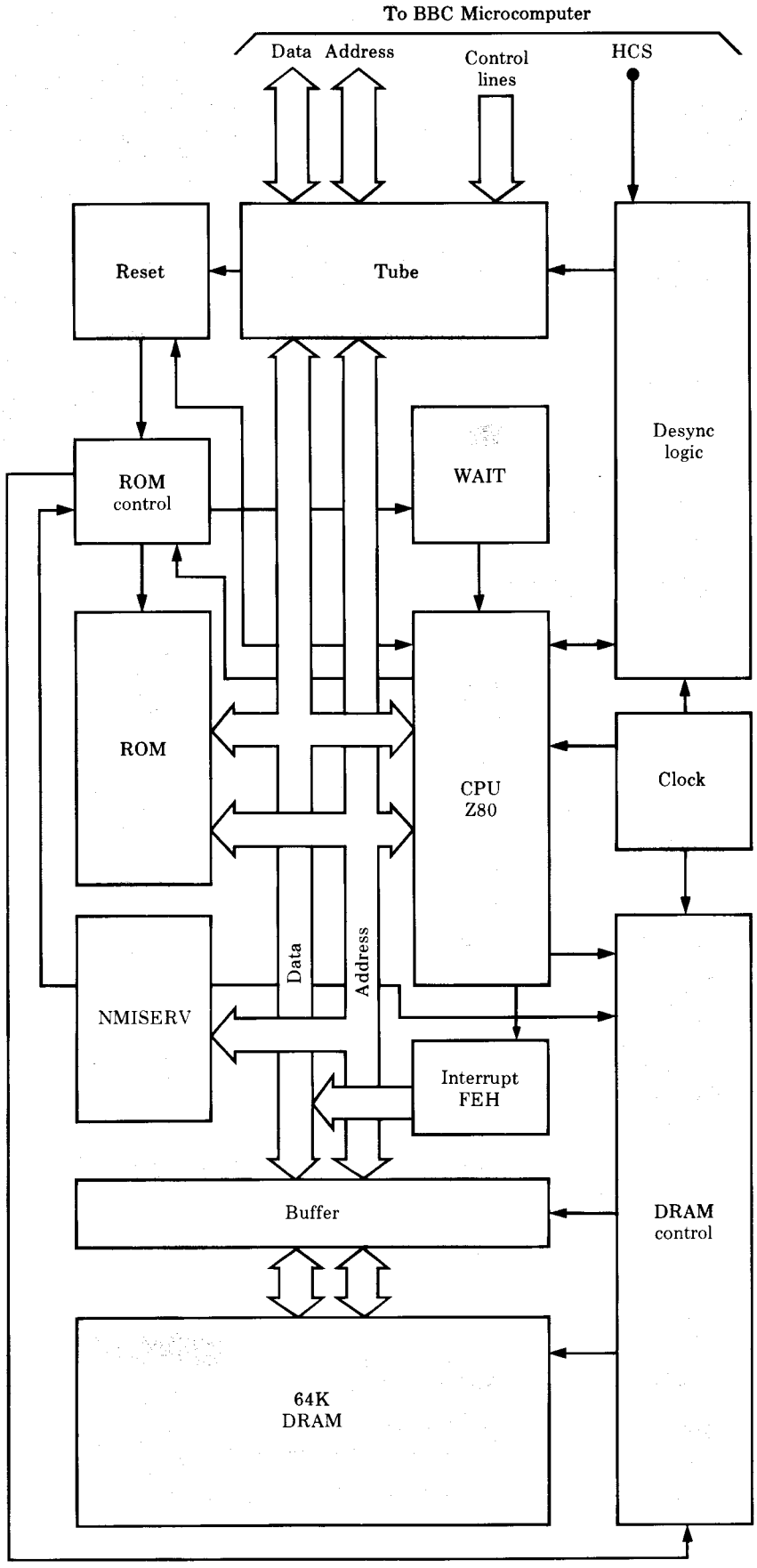

B
TUBE Z80 message displayed; no response to keyboard
Is DNFS ROM version 1.0?
Replace with DNFS ROM 1.0 or higher
Is current drawn by Z80 PCB > 800mA ?
Check for hot component and replace
Check for temperature-sensitive component failure
Any temperature-sensitive components found and replaced?
Check: Refresh circuits Address/data lines DRAMs
X


C
BBC Microcomputer 32K message displayed
Y
Is there 4.9–5.25V across C3?
E
Is there power on P4 of IC1 from BBC?
Is there power at BBC Tube socket?
Repair BBC Micro
Check ribbon cable assembly and connectors
Is power at pins 2 and 3 of Tube IC1?
Check tracks and L1/R2 for failure
Is there continuity from pin 6 of IC1 to pin 29 of ribbon connector and to BBC Micro?
Repair or replace
X

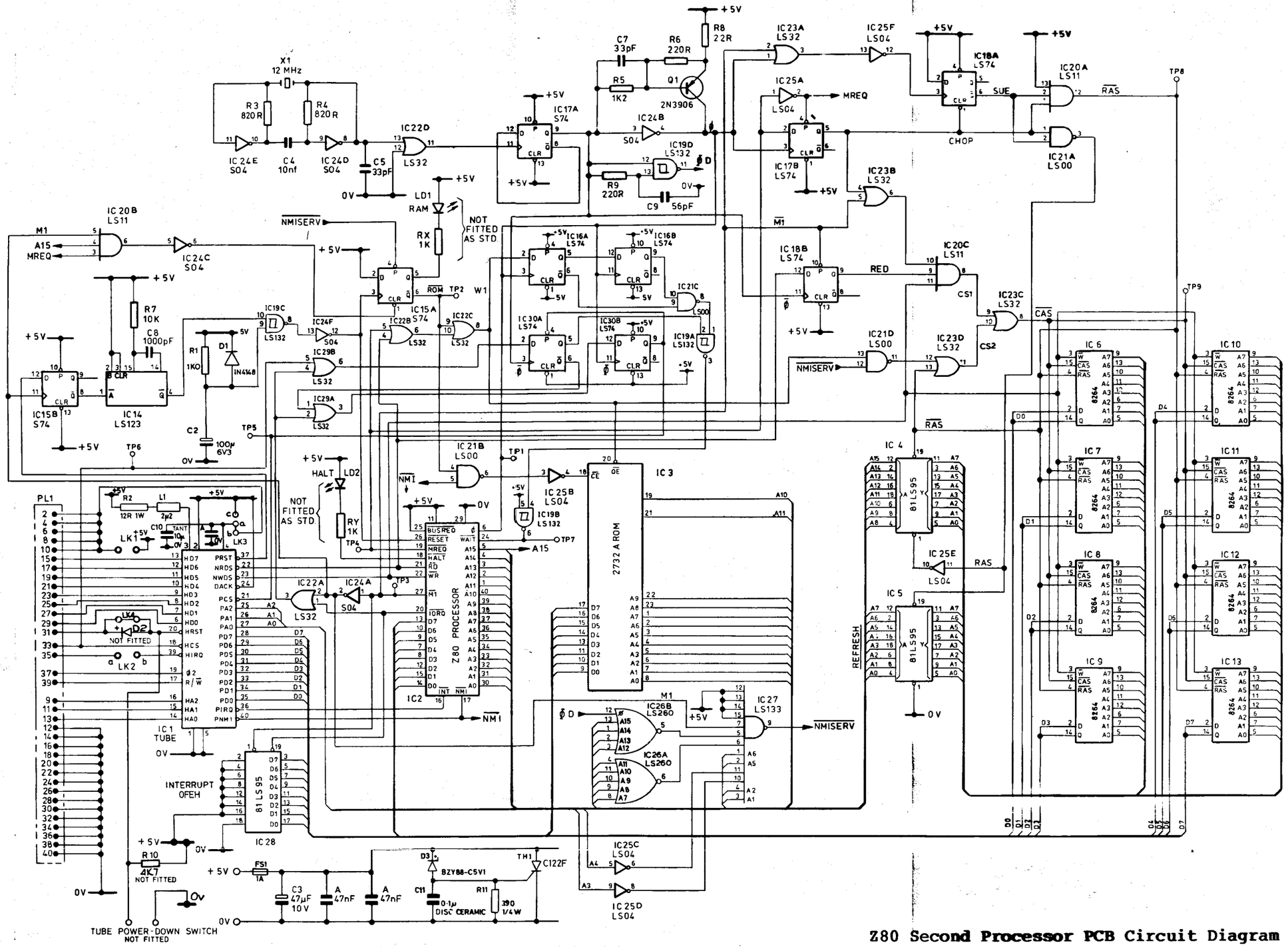

D
Flashing cursor displayed
Any damage to ribbon cable or connectors ?
✓
Repair/ replace as required
X
Any tracks broken or shorted?
✓
Repair as required
X
Is current drawn by Z80 PCB > 800mA?
✓
Check for:
Short circuit on supply rail
Hot component
X
Check the following circuits in sequence:
Clock
Power-up reset
Wait
ROM enable
Desync logic
Interrupt
RAS/CAS
DRAMs
Retest at each stage
X


E
Check 250mA mains fuse at rear of unit; replace if necessary
Check PSU, mains switch and wiring
Remove power supply leads from Z80 PCB, connect 10Ω 2.5W resistor across leads and measure voltage
Set +5V adjust potentiometer on PSU to give 5V with 50mV max noise
If unobtainable, replace PSU
Is voltage 4.9–5.1V with 50mV max noise?
Remove 10Ω resistor and reconnect to PCB
Measure current drawn by PCB
Fuse FS1 blown
Replace fuse; if fuse blows again check for and correct short on PCB
Look for and correct open circuit on Z80 PCB
Is voltage zero?
Measure voltage across C3
Any short circuit found and corrected?
Check for device which is hot and replace it
Check for and correct short circuit on PCB
Is current 700mA ± 100mA?
Is current zero?
Is current greater than 800mA?
Current is less than 700mA; check power rails to all ICs
Y

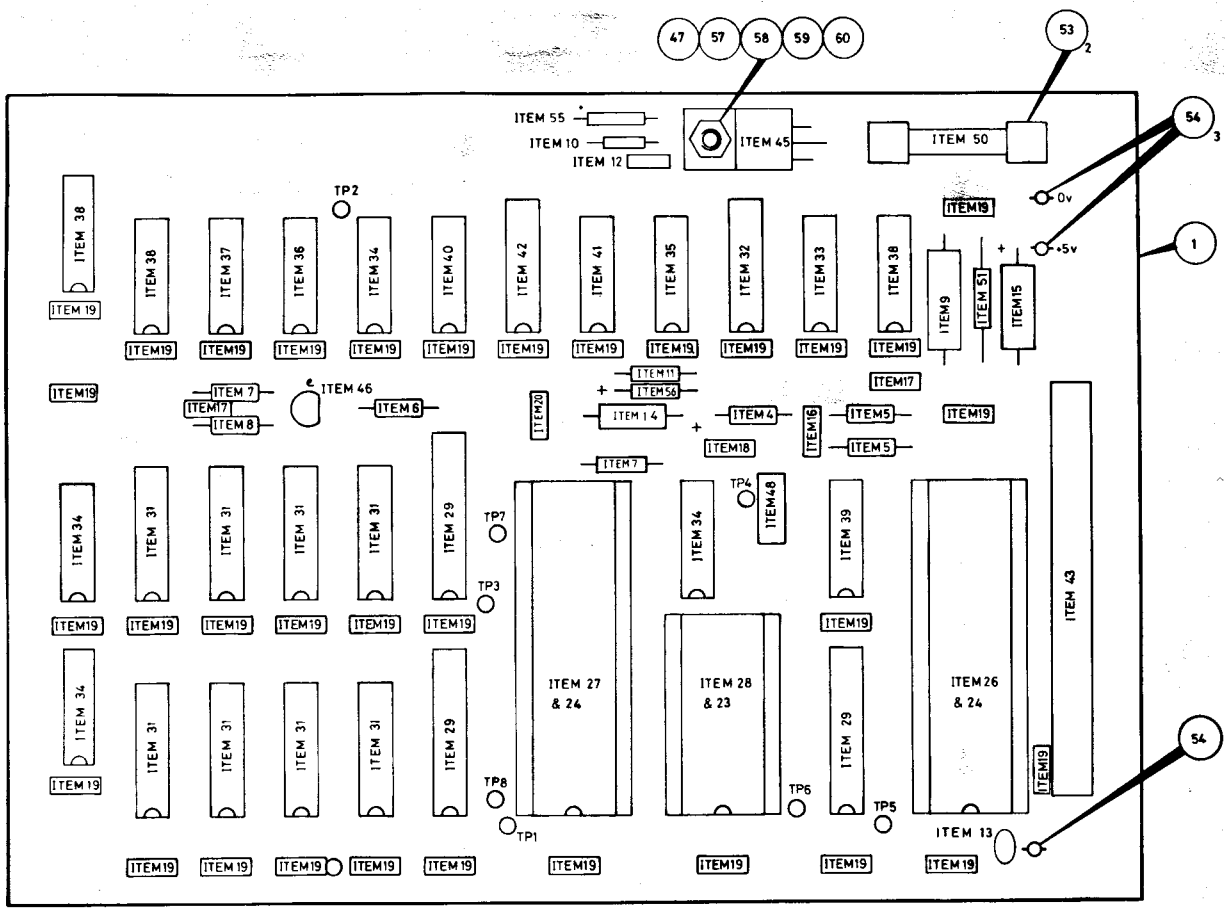


Z80 Second Processor Functional Block Diagram

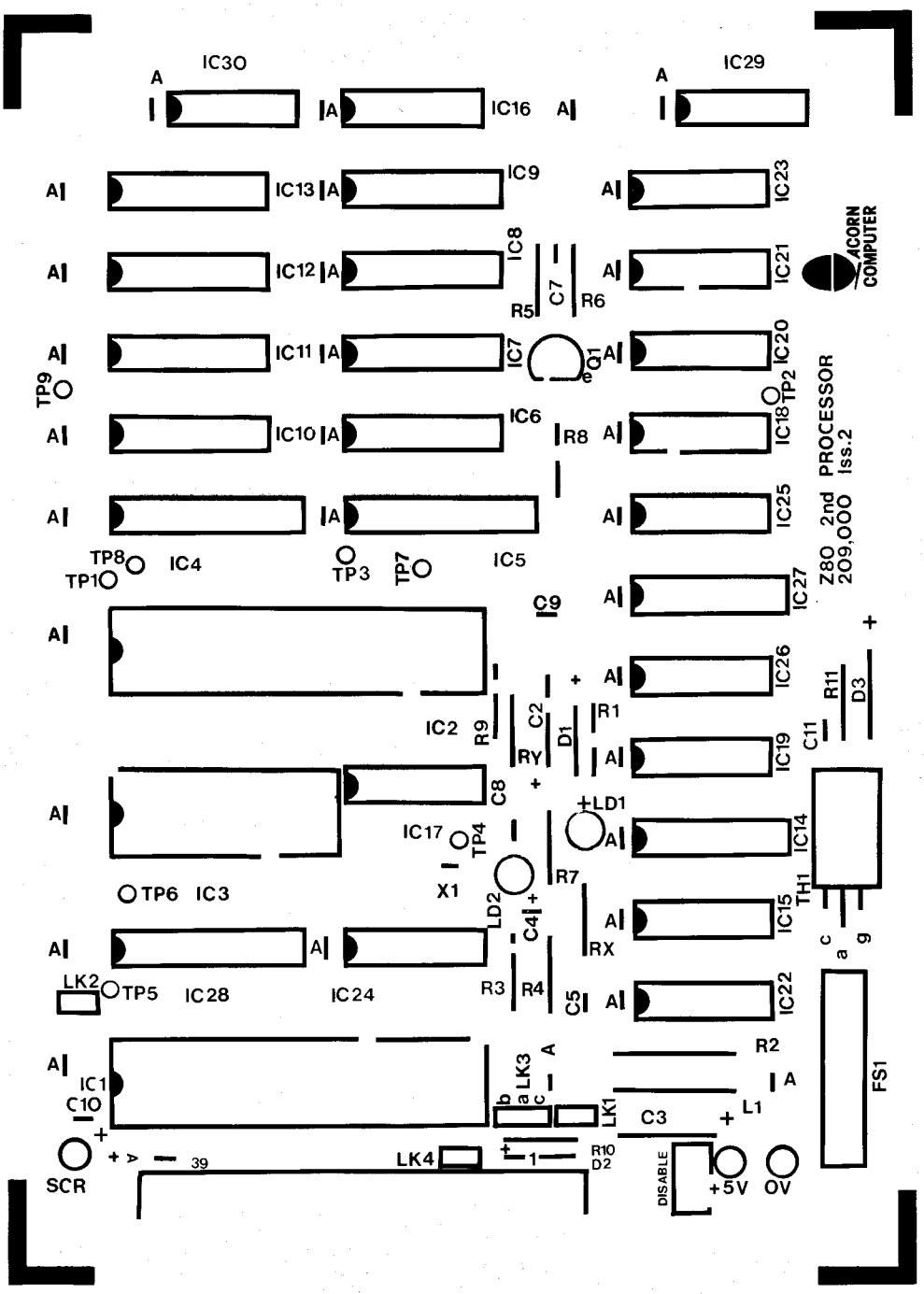
IC No	0V	+5V	TYPE No.
1			TUBE
2			Z80
3	12	24	2372
4	10	20	81LS95
5	10	20	81LS95
6	16	8	8264
7	16	8	8264
8	16	8	8264
9	16	8	8264
10	16	8	8264
11	16	8	8264
12	16	8	8264
13	16	8	8264
14	8	16	74LS123
15	7	14	74S74
16	7	14	74LS74
17	7	14	74S74
18	7	14	74LS74
19	7	14	74LS132
20	7	14	74LS11
21	7	14	74LS00
22	7	14	74LS32
23	7	14	74LS32
24	7	14	74LS04
25	7	14	74LS04
26	7	14	74LS260
27	7	14	74LS133
28	10	20	81LS95
29	7	14	74LS32
30	7	14	74LS74



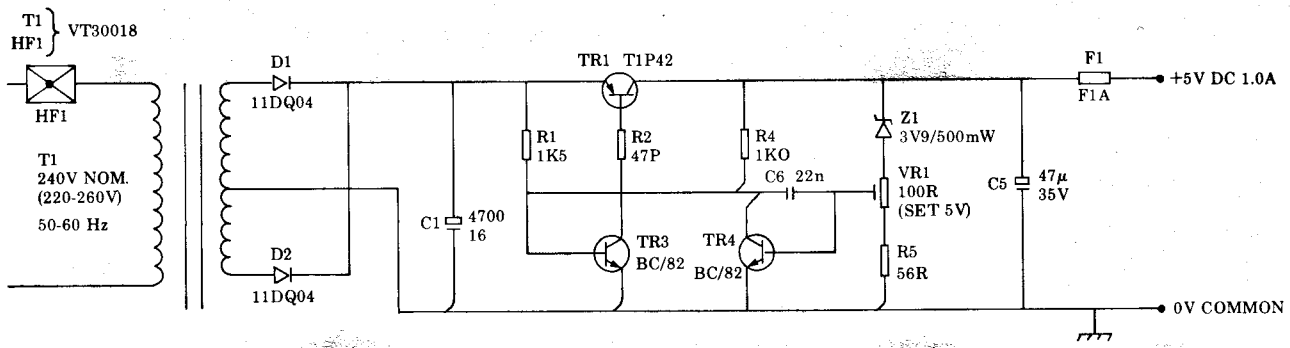
Z80 Second Processor PCB Circuit Diagram



Z80 PCB Component Layout



Z80 PCB Silk Screen



Power Supply Circuit Diagram

WARNING: THE Z80 SECOND PROCESSOR MUST BE EARTHED

Important: The wires in the mains lead for the Z80 second processor are coloured in accordance with the following code:

Green and yellow	**Earth**
Blue	**Neutral**
Brown	**Live**

As the colours of the wires may not correspond with the coloured markings identifying the terminals in your plug, proceed as follows:

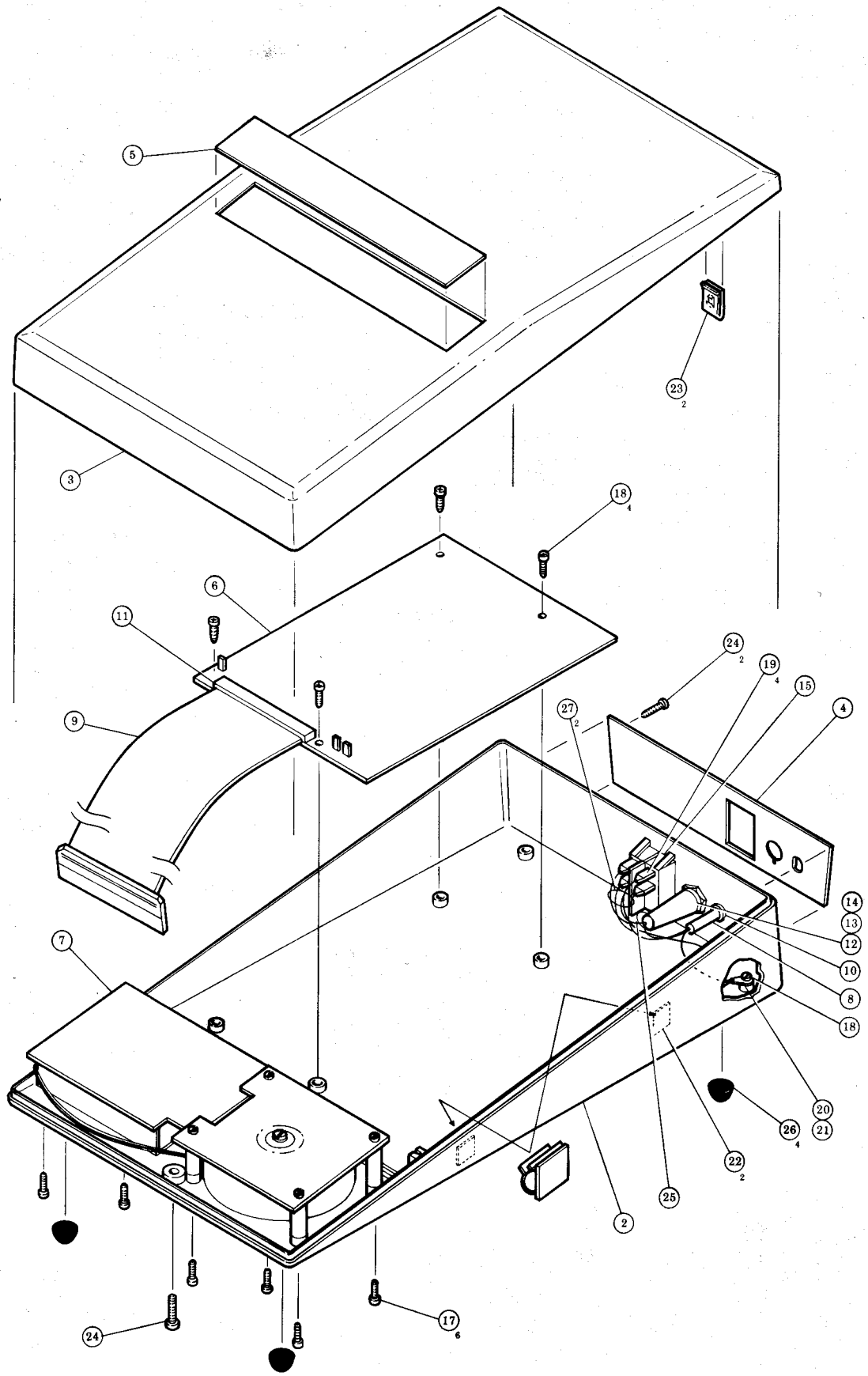
The wire which is coloured green and yellow must be connected to the terminal in the plug which is marked by the letter E, or by the safety earth symbol ⏚ or coloured green, or green and yellow.

The wire which is coloured blue must be connected to the terminal which is marked with the letter N, or coloured black.

The wire which is coloured brown must be connected to the terminal which is marked with the letter L, or coloured red.

If the socket outlet available is not suitable for the plug supplied, the plug should be cut off and the appropriate plug fitted and wired as previously noted. The moulded plug which was cut off must be disposed of as it would be a potential shock hazard if it were to be plugged in with the cut off end of the mains cord exposed. The moulded plug must be used with the fuse and fuse carrier firmly in place. The fuse carrier is of the same basic colour* as the coloured insert in the base of the plug. Different manufacturers' plugs and fuse carriers are not interchangeable. In the event of loss of the fuse carrier, the moulded plug MUST NOT be used. Either replace the moulded plug with another conventional plug wired as previously described, or obtain a replacement fuse carrier from an authorised BBC Microcomputer dealer. In the event of the fuse blowing it should be replaced, after clearing any faults, with a 3 amp fuse that is ASTA approved to BS1362.

*Not necessarily the same shade of that colour.



Z80 Second Processor General Assembly

Z80 Second Processor Parts Lists

NOTE: Items indentified by * are normally available as spare parts - please contact your supplier for details of availability.

ITEM	PART No.	DESCRIPTION	QTY	REMARKS
Z80 Second Processor General Assembly (SEE PAGE 47)				
2	201,110 *	CASE LOWER MOULDING	1	
3	201,109 *	CASE UPPER MOULDING	1	
4	201,742 *	CASE LABEL, LOWER	1	(REAR)
5	201,108 *	CASE LABEL UPPER	1	
7	831,000 *	POWER SUPPLY ASSEMBLY	1	
8	870,302	MAINS CABLE C/W PLUG	1	
9	870,040 *	40 WAY RIBBON CABLE, GREY 260mm	1	
	800,027 *	40 WAY RIBBON CABLE STRAIN RELIEF	1	
	800,017 *	40 WAY RIBBON CABLE CABLE SOCKET	1	
10	880,025	CABLE GROMMET	1	
11	800,037 *	S.H.E. CONNECTOR	1	TOP HALF
12	815,900	FUSE HOLDER	1	
13	815,901	FUSE HOLDER SHROUD	1	
14	815,207 *	FUSE 20mm x 5mm 250mA TYPE T	1	SLO BLO
15	805,003 *	MAINS SWITCH	1	
23	882,946 *	SPIRE NUT No.6	2	
24	882,665	SELFTAP PAN HD SCREW No6 x 13mm	3	BLACK
26	890,000 *	'STICK-ON' FOOT	4	
Z80 PCB Assembly (SEE PAGE 41)				
4	502,103	RESISTOR 10K 1/4W 5%	1	R7
5	502,821	RESISTOR 820R 1/4W 5%	2	R3,4
6	502,220	RESISTOR 22R 1/4W 5%	1	R8
7	502,221	RESISTOR 220R 1/4W 5%	2	R6,9
8	502,122	RESISTOR 1K2 1/4W 5%	1	R5
9	502,120	RESISTOR 12R 1W 10%	1	R2
10	502,391	RESISTOR 390R 1/4W 5%	1	R11
11	502,102	RESISTOR 1K 1/4W 5%	1	R1
12	628,101	CAPACITOR 100nF CERAMIC	1	C11
13	613,101	CAPACITOR 10uF 35V TANT	1	C10
14	620,101	CAPACITOR 100uF 6V3 ELEC	1	C2
15	621,470	CAPACITOR 47uF 10V ELEC	1	C3
16	629,010	CAPACITOR 10nF PLATE CERAMIC	1	C4
17	631,033	CAPACITOR 33pF PLATE CERAMIC	2	C5,7
18	630,100	CAPACITOR 1000pF PLATE CERAMIC	1	C8
19	628,470	CAPACITOR, DECOUPLER	33	A NOM.47nF
20	631,056	CAPACITOR 56pF PLATE CERAMIC	1	C9
23	800,124 *	IC SOCKET 24 WAY DIL	1	FOR IC3
24	800,140 *	IC SOCKET 40 WAY DIL	2	FOR IC1,2
26	201,605 *	INTEGRATED CIRCUIT TUBE	1	IC1
27	700,080 *	INTEGRATED CIRCUIT Z80B	1	IC2 CPU
28	201,644 *	INTEGRATED CIRCUIT, BOOT ROM	1	IC3
29	738,095 *	INTEGRATED CIRCUIT 81LS95/74LS795	3	IC4,5,28

Z80 PCB Assembly (SEE PAGE 41) - cont'd

31	704,164 *	INTEGRATED CIRCUIT 8264	8	IC6-13
32	742,123 *	INTEGRATED CIRCUIT 74LS123	1	IC14
33	741,074/ 748,074 *	INTEGRATED CIRCUIT 74S74/74F74	2	IC15
34	742,074 *	INTEGRATED CIRCUIT 74LS74	3	IC16-18,30
35	742,132 *	INTEGRATED CIRCUIT 74LS132	1	IC19
36	742,011 *	INTEGRATED CIRCUIT 74LS11	1	IC20
37	742,000 *	INTEGRATED CIRCUIT 74LS00	1	IC21
38	742,032 *	INTEGRATED CIRCUIT 74LS32	3	IC22,23,29
39	741,004 *	INTEGRATED CIRCUIT 74S04	1	IC24
40	742,004 *	INTEGRATED CIRCUIT 74LS04	1	IC25
41	742,260 *	INTEGRATED CIRCUIT 74LS260	1	IC26
42	742,133 *	INTEGRATED CIRCUIT 74LS133	1	IC27
43	800,037 *	S.H.E. CONNECTOR	1	PL1 (HALF)
45	791,000	THYRISTOR C122F	1	TH1
46	783,906 *	TRANSISTOR 2N3906	1	Q1
47	880,049	INSULATOR	1	FOR ITEM 45
48	820,120 *	CRYSTAL 12MHz	1	X1
50	815,007 *	FUSE 20mm x 5mm 1 AMP	1	FS1
51	860,002 *	INDUCTOR 2u2 10%	1	L1
53	815,910	FUSE CLIP	2	
54	800,200	FASTON TAB	3	
55	795,006	DIODE ZENER BZY88 - C5V1	1	D3
56	794,148	DIODE 1N4148	2	D1

1. Introduction

This manual is intended to provide the information required to diagnose and repair faults on the Z80 second processor (a part of the BBC Microcomputer system) which was designed by Acorn Computers Ltd. of Cambridge, England.

The information contained in this manual is aimed at Acorn dealers and service engineers who will be servicing the Z80 second processor on behalf of Acorn Computers Ltd.

Z80 is a trademark of Zilog Inc.
CP/M® is a registered trademark of Digital Research Inc.
The Tube is a trademark of Acorn Computers Limited.

2. Packaging and Installation.

The Z80 second processor is supplied in a two-part moulded polystyrene packing which is further packaged within a cardboard sleeve. Supplied with the second processor is a DNFS ROM with fitting instruction sheet, a set of reminder cards for the red function keys, 7 floppy disks, an end-user licence and a guarantee card. For BBC Microcomputers fitted with MOS ROMs below version 1.2, a voucher redeemable against replacement of lower version ROMs, is also supplied.

Note: Care should be taken when unpacking and repacking this unit to ensure that all items are positioned correctly, especially the floppy disks which should first be packed in plastic bags and laid flat.

The Z80 Second Processor User Guide and accompanying literature is supplied packed separately.

A mains power switch is located at the rear of the second processor.

A 250mA. type T (slow blow) fuse is located at the rear of the second processor. Before removing this fuse, the second processor must be disconnected from the mains supply. Access to the fuse may be gained by undoing the round cover with the slot in it using a screwdriver. The mains supply must not be reconnected until the fuse is relocated in its holder with the cover screwed home.

Do not use the second processor in conditions of extreme heat, cold, humidity or dust, or in places subject to vibration. Do not block the ventilation under or behind the second processor. Ensure that no foreign objects are inserted through any openings in the second processor.

3. Specification

3.1 The Z80 second processor

A second processor for the BBC Microcomputer model B, operating through the Tube, providing the ability to run sophisticated software under the CP/M 2.2 operating system.

The second processor is housed in a rigid injection moulded thermoplastic case and contains the following:

A 6MHz Z80B CPU

64K of read/write Random Access Memory

4K Read Only Memory ("shadow ROM") providing a boot function on power-up and to handle Non-Maskable Interrupts (NMI) from the Host processor via the Tube.

The Tube - a fast asynchronous communication path connecting the second processor to the I/O processor (BBC Microcomputer).

A mains-operated integral power supply comprising a mains transformer and power supply board.

3.2 Power Supply

Max. AC Input	264V AC
MIN. AC Input	216V AC
Power Rating	14 watts
Supply Frequency	47-63Hz
Max. Output Current	1A at +5V

4. Disassembly and assembly

To service the Z80 second processor, disconnect it from the BBC Microcomputer and the mains supply and undo the three fixing screws; two at the top of the back panel and one underneath the unit, nearest the front and equidistant between the two rubber feet. (The assembly diagram is given in the Appendix). The lid can now be removed revealing the transformer and power supply board, held in place by six screws, and the Z80 PCB. It is recommended that the transformer and power supply board are not removed unless absolutely necessary.

To remove the Z80 PCB from the case, pull off the two "fast on" tabs which connect the power supply (brown +5v and black 0v leads) and remove the four screws which hold the PCB in place.

5. Circuit Description

The circuit may be split into a number of sections by their specific function. These are dealt with under separate headings. Reference should be made, where necessary, to the block diagram and circuit diagram in the appendix.

5.1 CPU

The microprocessor used in this unit is a Z80B, running at a clock frequency of 6MHz from a crystal oscillator. All memory and I/O cycles are performed at full speed, with the exception of those to the "boot" ROM, for which a Wait-State is inserted by external logic.

5.2 Clock

A 12MHz crystal controls the frequency of the oscillator formed by the inverters IC 24D,E. A "D" type latch, IC17A, is used to divide the frequency to the required 6MHz. Transistor Q1 provides an active pull-up for the clock signal, after inversion by IC 24B, to compensate for the high dynamic input current of the Z80 on this signal. The NAND gate IC19D and associated network , provide a shaped clock signal for the "NMI Service Detect" logic. Since the output of the "D" latch is inverted before being used as CPU clock, then the "D" output is available for use as an inverted clock by the DRAM control and the desync. logic.

5.3 ROM Latch

The Z80 second processor features a "shadow" ROM to boot the system upon power-up and also to ensure proper handling of NMI interrupts from the host processor via The Tube. The ROM is enabled at the proper times by the latch IC15A.

1. After power-up, the reset signal from IC24F to the Z80 is used to clock the latch IC15A and produce the ROM signal. On any memory read cycle, while the Rom signal (TP2) is active, IC22B&C will produce an output-enable signal to the ROM (IC3 pin 20).

The initial instructions following RESET are executed from ROM and initiate the copying of ROM into high RAM. This is followed by an instruction-fetch cycle to memory over 8000H which is detected by the AND gate IC20B and used to clear the ROM latch, remove the shadow ROM from the memory-map, and allow normal running in RAM.

2. The NMI signal to the Z80 processor is used by system software in Disc handling, however, the Z80 interrupt vector to 66H is not compatible with standard CPM, which has its default file-control block in this area. The solution used is to bring the shadow ROM temporarily into the memory-map when an instruction fetch from 66H

Acorn Computers Limited, Fulbourn Road, Cherry Hinton, Cambridge CB1 4JN, England